The ***ICECUBE_DP++TX*** PHY is a VESA Dual-mode DisplayPort **(DisplayPort++)** Transmitter

DP++ is a standard for transmission of digital audio/video (A/V) signals from different audiovisual sources to television sets, projectors and other video displays.

It can carry all standard and high-definition consumer electronics video formats as well as high quality multi-channel audio data.

DP++ can also carry control and status information in both directions. The ***ICECUBE_DP++TX*** PHY is embedded in SoC's that require transmission of high-speed audiovisual data following the HDMI 2.0 and DisplayPort 1.2 standards.

Supported Standards

- Dual-Mode DisplayPort 1.1 (DP++)
- DisplayPort 1.1/1.2
- HDMI 1.3/1.4 (AC-Coupled and/or DC-Coupled with external passive components)
- HDMI 2.0 (AC-Coupled and/or DC-Coupled with external passive components

Fabrication Technology

- Process - TSMC 28nm HPM
  0.9V core voltage, 2.5V IO devices, 1.8V optional/modifications
- Poly Orientation – Vertical
- Metallization – 1p10m_5x2y2r_alrdl
- Designed for FlipChip (Wire-Bond optional)
- Bumping pitch - Drawn = 187.38 µm, Silicon = 168.65 µm
- Special Masks: Deep N-Well and LVT

Macro Size

- Drawn
  - Ultra-Small area = (Under NDA) mm^2
  - Height = (Under NDA) µm; Width = (Under NDA) µm
- Silicon
  - Area = (Under NDA) mm^2
  - Height = (Under NDA) µm; Width = (Under NDA) µm

Macro Power Consumption

- Typical: (Under NDA) mW (VDDA=0.9V; VDDH=3.3V/2.5V) @ 6Gbps/Lane (HDMI)

Contact us: Gennady Burdo; office: +972-72-2223917; email: gennady@uni-phy.com

Deliveries

- GDSII
- LVS Netlist
- LEF
- .LIB
- Verilog Behavioral model
- Integration guidelines
- Configuration Software
- Compliance Report

Special Features

- Programmable 3-Tap FIR TX Equalizer
- Each Lane can be configured as TMDS clock lane in HDMI mode
- 32 bits wide parallel interface
- Clocking support for DisplayPort ↔ HDMI mapping and wise versa
- Optional SSC filtering in DisplayPort → HDMI mapping mode
- Optional SSC generation in DisplayPort mode
- Low Power consumption
- Small Area

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