

Failure-free Coordinator Synthesis for Correct Components Assembly

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ABSTRACT

One of the main challenges in components assembly is related to the ability to predict possible coordination policies of the components interaction behavior by only assuming a limited knowledge of the single components computational behavior. Our answer to this problem is a software architecture based approach in which the software architecture imposed on the coordinating part of the system, allows for detection and recovery of COTS (*Commercial-Off-The-Shelf*) concurrency conflicts and for the enforcing of coordination policies on the interaction behavior of the components into composed system. Starting from the specification of the system to be assembled and of the coordination policies for the components interaction behavior, we develop a framework which automatically derives the glue code for the set of components in order to obtain a conflict-free and coordination policy-satisfying system.

1. INTRODUCTION

One of the main challenges in components assembly is related to the ability to predict possible coordination policies of the components interaction behavior by only assuming a limited knowledge of the single components computational behavior. Our answer to this problem is a software architecture based approach [15, 14] in which the software architecture imposed on the coordinating part of the system, allows for detection and recovery of COTS (*Commercial-Off-The-Shelf*) [23] concurrency conflicts and for the enforcing of coordination policies on the interaction behavior of the components into composed system. Building a system from a set of COTS components introduces problems related to their truly black-box nature. Since system developers have no method of looking inside the box, they can only operate on components interaction behavior to enforce coordination policies of the components into assembled system. In this context, the notion of software architecture assumes a key role since it represents the reference skeleton used to com-

pose components and let them interact. In the software architecture domain, the interaction among the components is represented by the notion of software connector [2]. We recall that a software architecture is defined as *"the structure of the components of a system, their interrelationships, principles and guidelines governing their design and evolution over time, plus a set of connectors that mediate communication, coordination or cooperation among components."* [9].

Our approach is to compose systems by assuming a well defined architectural style [15] in such a way that it is possible to detect and to fix software anomalies. An architectural style is defined as *"a set of constraints on a software architecture that identify a class of architectures with similar features"* [4]. Moreover we assume that a specification of the desired assembled system is available and that a precise definition of the coordination policies to enforce exists. With these assumptions we are able to develop a framework that automatically derives the assembly code for a set of components so that, if possible, a conflict-free and coordination policy-satisfying system is obtained. The assembly code implements an explicit software connector (i.e. a coordinator) which mediates all interactions among the system components as a new component to be inserted in the composed system. The connector can then be analyzed and modified in such a way that the concurrency conflicts can be avoided and the specified coordination policies can be enforced on the interaction behavior of the others components into assembled system. Moreover the software architecture imposed on the composed system allows for easy replacement of a connector with another one in order to make the whole system flexible with respect to different coordination policies.

In previous works [15, 14] we limited ourselves to only concurrency conflict avoidance by enforcing only one type of coordination policy namely deadlock-free policy. In [13] we have applied the deadlock-free approach in a real scale context, namely the context of COM/DCOM applications. In this paper we generalize the framework by addressing generic coordination policies of the components into assembled system. In other works [17, 16] we have applied the framework we show in this paper to an instance of a typical CSCW (*Computer Supported Cooperative Work*) application, that is a collaborative writing (CW) system we have designed.

The paper is organized as follows. Sections 2 and 3 introduce

background notions and, by using an explanatory example, summarize the method concerning the synthesis of coordinators that are only deadlock-free, already developed in [15, 14]. Section 3.3 contains the main contribution of the paper and, by continuing the explanatory example, formalizes the conflict-free coordination policy-satisfying connectors synthesis. Section 4 presents related works and Section 5 discusses future work and concludes.

2. BACKGROUND

In this section we provide the background needed to understand the approach formalized in Sections 3 and 3.3.

2.1 The reference architectural style

The architectural style we use, called *Connector Based Architecture* (CBA), consists of components and connectors which define a notion of top and bottom. The top (bottom) of a component may be connected to the bottom (top) of a single connector. Components can only communicate via connectors. It is disallowed the direct connection between connectors. Components communicate synchronously by passing two type of messages: notifications and requests. A notification is sent downward, while a request is sent upward. A top-domain (bottom-domain) of a component or of a connector is the set of requests sent upward and of received notifications (of received requests received and of notifications sent downward). Connectors are responsible for the routing of messages and they exhibit a strictly sequential input-output behavior¹. The CBA style is a generic layered style. For the sake of presentation, in this paper we describe our approach for single-layer systems. In [15] we show how to cope with multi-layered systems.

2.2 Configuration formalization

To our purposes we need to formalize two different ways to compose a system. The first one is called *Connector Free Architecture* (CFA) and is defined as a set of components directly connected in a synchronous way (i.e. without a connector). The second one is called *Connector Based Architecture* (CBA) and is defined as a set of components directly connected in a synchronous way to one or more connectors. In order to describe components and system behaviors we use CCS [19] (*Calculus of Communicating Systems*) notation. For the purpose of this paper this is an acceptable assumption. Actually our framework allows to automatically derive these CCS descriptions from "HMSC (*High level Message Sequence Charts*)" and "bMSC (*basic Message Sequence Charts*)" [1] specifications of the system to be assembled [21, 16]. This derivation step is performed by applying a suitable version of a translation algorithm from bMSCs and HMSCs to LTS (*Labelled Transition Systems*) [26]. HMSC and bMSC specifications are common practice in real-scale contexts thus CCS can merely be regarded as an internal to the framework specification language. Since these specifications model finite-state behaviors of a system we will use finite-state CCS:

Definition 1. Connector Free Architecture (CFA):

$CFA \equiv (C_1 | C_2 | \dots | C_n) \setminus \bigcup_{i=1}^n Act_i$ where for all $i = 1, \dots, n$, Act_i is the actions set of the CCS process C_i .

¹Each input action is strictly followed by the corresponding output action.

Definition 2. Connector Based Architecture (CBA):
 $CBA \equiv (C_1[f_1] | C_2[f_2] | \dots | C_n[f_n] | K) \setminus \bigcup_{i=1}^n Act_i[f_i]$ where for all $i = 1, \dots, n$, Act_i is the actions set of the CCS process C_i and f_i is a relabelling functions such that $f_i(\alpha) = \alpha_i$ for all $\alpha \in Act_i$ and K is the CSS process representing the connector.

In Figure 1 we show an example of CFA system and of the corresponding CBA system. The double circled states represent initial states.

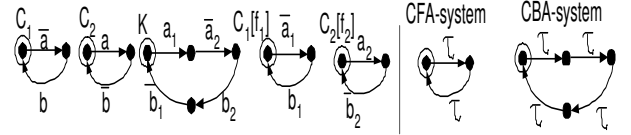


Figure 1: CFA and corresponding CBA

3. APPROACH DESCRIPTION

The problem we want to treat can be informally phrased as follows: given a CFA system T for a set of black-box interacting components and a set of coordination policies P automatically derive the corresponding CBA system V which implements every policy in P .

We are assuming that a specification of the system to be assembled is provided. Referring to Definition 1, we assume that for each component a description of its behavior as finite-state CCS term is provided (i.e. LTS *Labelled Transitions System*). Moreover we assume that a specification of the coordination policies to be enforced exists. In the following, by means of a working example, we discuss our method proceeding in three steps as illustrated in Figure 2.

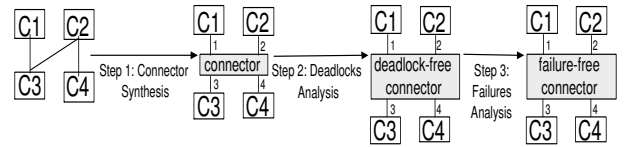


Figure 2: 3 step method

The first step builds a connector (i.e. the coordinator) following the CBA style constraints. The second step performs the concurrency conflicts (i.e. deadlocks) detection and recovery process. Finally, the third step performs the enforcing of the specified coordination policies against the conflict-free connector and then synthesizes a coordination policy-satisfying connector. The firsts two steps concern the approach already developed in our precedent works [15, 14]. Instead the third step concerns the extension of the approach to deal with generic coordination policy. From the latter we can derive the code implementing the coordinator component which is by construction correct with respect to the coordination policies specification.

Note that although in principle we could carry on the second and third step together we decided to keep them separate. Actually, the current framework implementation follows this schema.

3.1 First step: Coordinator Synthesis

The first step of our method (see Figure 2) starts with a CFA system and produces the equivalent CBA system. It is worthwhile noticing that this can always be done [15]. We proceed as follows:

i) for each finite-state CCS component specification in the CFA system we derive the corresponding AC-Graph. AC-Graphs model components behavior in terms of interactions with the external environment. AC-Graph carry on information on both labels and states:

Definition 3. AC-Graph:

Let $\langle S_i, L_i, \rightarrow_i, s_i \rangle$ be a labelled transition system of a component C_i . The corresponding Actual Behavior (AC) Graph AC_i is a tuple of the form

$\langle N_{AC_i}, LN_{AC_i}, A_{AC_i}, LA_{AC_i}, s_i \rangle$ where $N_{AC_i} = S_i$ is a set of nodes, LN_{AC_i} is a set of state labels, LA_{AC_i} is a set of arc labels with τ ($LA_{AC_i} = L_i \cup \tau$), $A_{AC_i} \subseteq N_{AC_i} \times LA_{AC_i} \times N_{AC_i}$ is a set of arcs and s_i is the root node.

- We shall write $g \xrightarrow{l} h$, if there is an arc $(g, l, h) \in A_{AC_i}$. We shall also write $g \rightarrow h$ meaning that $g \xrightarrow{l} h$ for some $l \in LA_{AC_i}$.
- If $t = l_1 \dots l_n \in LA_{AC_i}^*$, then we write $g \xrightarrow{t} h$, if $g \xrightarrow{l_1} \dots \xrightarrow{l_n} h$. We shall also write $g \xrightarrow{*} h$, meaning that $g \xrightarrow{t} h$ for some $t \in LA_{AC_i}^*$.
- We shall write $g \xRightarrow{l} h$, if $g \xrightarrow{t} h$ for some $t \in \tau^*.l.\tau^*$.

In Figure 3 we show the AC-Graphs of the CFA system of our explanatory example. The double-circled states are the initial states. For the transition labels we use a CCS notation (α is an input action and $\bar{\alpha}$ is the corresponding output action).

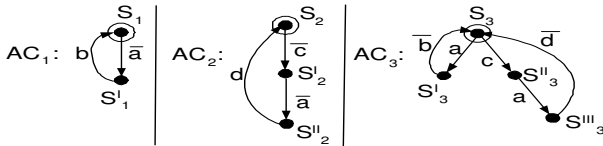


Figure 3: AC-Graphs of the example

We are assuming a client-server components setting. AC_1 and AC_2 are the AC-Graphs of the two client components (i.e. C_1 and C_2). AC_3 is the AC-Graph of the server component (i.e. C_3). C_3 exports two services, namely a and c . c has not a return value. a has either b or d as return values. The input actions on AC_3 represent requests of service from the clients while the output actions represent return values towards the clients. The input actions on AC_1 and AC_2 represent return values from the server while the output actions represent requests of service towards the server.

ii) We derive from AC-Graph the requirements on its environment that guarantee concurrency conflict (i.e. deadlock)

freedom. Referring to Definition 1, the environment of a component C_i is represented by the set of components C_j ($j \neq i$) in parallel. A component will not be in conflict with its environment if the environment can always provide the actions it requires for changing state. This is represented as AS-Graphs (Figure 4):

Definition 4. AS-Graph:

Let $(N_{AC_i}, LN_{AC_i}, A_{AC_i}, LA_{AC_i}, s_i)$ be the AC-Graph AC_i of a component C_i , then the corresponding ASumption (AS) Graph AS_i is $(N_{AS_i}, LN_{AS_i}, A_{AS_i}, LA_{AS_i}, s_i)$ where $N_{AS_i} = N_{AC_i}$, $LN_{AS_i} = LN_{AC_i}$, $LA_{AS_i} = LA_{AC_i}$ and $A_{AS} = \{(\nu, \bar{a}, \nu') \mid (\nu, a, \nu') \in A_{AC}\} \cup \{(\nu, b, \nu') \mid (\nu, \bar{b}, \nu') \in A_{AC}\}$.

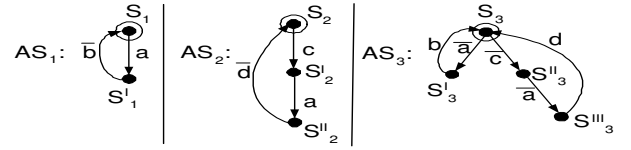


Figure 4: AS-Graphs of the example

Now if we consider Definition 2, the environment of a component can only be represented by connectors, EX-Graph represents the behavior that the component expects from the connectors (Figure 5):

Definition 5. EX-Graph: Let $(N_{AS_i}, LN_{AS_i}, A_{AS_i}, LA_{AS_i}, s_i)$ be the AS-Graph AS_i of a component C_i ; we define the connector EXpected (EX) Graph EX_i from the component C_i the graph $(N_{EX_i}, LN_{EX_i}, A_{EX_i}, LA_{EX_i}, s_i)$, where:

- $N_{EX_i} = N_{AS_i}$ and $LN_{EX_i} = LN_{AS_i}$
- A_{EX_i} and LA_{EX_i} are empty
- $\forall (\mu, \alpha, \mu') \in A_{AS_i}$, with $\alpha \neq \tau$
 - Create a new node μ_{new} with a new unique label, add the node to N_{EX_i} and the unique label to LN_{EX_i}
 - if (μ, α, μ') is such that α is an input action (i.e. $\alpha = a$, for some a)
 - * add the labels a_i and $\bar{a}_?$ to LA_{EX_i}
 - * add (μ, a_i, μ_{new}) and $(\mu_{new}, \bar{a}_?, \mu')$ to A_{EX_i}
 - if (μ, α, μ') is such that α is an output action (i.e. $\alpha = \bar{a}$, for some a)
 - * add the labels $\bar{a}_?$ and $a_?$ to LA_{EX_i}
 - * add $(\mu, a_?, \mu_{new})$ and $(\mu_{new}, \bar{a}_?, \mu')$ to A_{EX_i}
- $\forall (\mu, \tau, \mu') \in A_{AS_i}$ add τ to LA_{EX_i} and (μ, τ, μ') to A_{EX_i}

iii) Each EX-Graph represents a partial view (i.e. the single component's view) of the connector behavior. The EX-Graph for component C_i (i.e. EX_i) is the behavior that C_i expects from the connector. Thus EX_i has either transitions

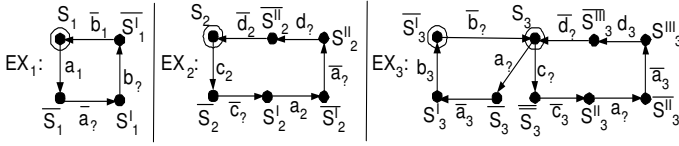


Figure 5: EX-Graphs of the example

labelled with known actions or with unknown actions for C_i . Known actions are performed on the channel connecting C_i to the connector. This channel is known to C_i and identified by a number. Unknown actions are performed on channels connecting other components C_j ($j \neq i$) to the connector, therefore unknown from the C_i perspective. These channels are identified by the question mark. We derive the connector global behavior through the following EX-Graphs unification algorithm.

Definition 6. EX-Graphs Unification:

- Let C_1, \dots, C_n be the components in CFA-version of the composed system in such a way that $\{C_1, \dots, C_h\}$ is the set of null bottom domain components and $\{C_{h+1}, \dots, C_n\}$ is the set of null top domain components;
- Let $EX_1, \dots, EX_h, EX_{h+1}, \dots, EX_n$ be their corresponding EX-Graphs;
- Let $1, \dots, h, h+1, \dots, n$ be their corresponding communication channels;
- Let $S_1, \dots, S_h, S_{h+1}, \dots, S_n$ be their corresponding current states.

At the beginning the current states are the initial states.

1. Create the actual behavior graph of the connector, with one node (initial state) and no arcs.
2. Set as current states of the components $EX - Graphs$ the respective initial states.
3. Label the connector initial state with an ordered tuple composed of the initial states of all components (null bottom domain and null top domain). For simplicity of presentation we assume to order them so that the j -th element of the state label corresponds to the current state of the component C_j where $j \in [1, \dots, h, h+1, \dots, n]$. This state is set as the connector current state.
4. Perform the following unification procedure:
 - (a) Let g be the connector current state. Mark g as visited.
 - (b) Let $\langle S_1, \dots, S_h, S_{h+1}, \dots, S_n \rangle$ be the state label of g .
 - (c) Generate the set TER of action_terms and the set VAR of action_variables so that $t_i \in TER$, if in EX_i $S_i \xrightarrow{t_i} \bar{S}_i$. Similarly $v_j \in VAR$, if $\exists j$ in such a way that in EX_j $S_j \xrightarrow{v_j} \bar{S}_j$.

- (d) For all unifiable pairs (t_i, v_j) , with $i \neq j$ do:
 - i. if $i \in \{1, \dots, h\}$, $j \in \{h+1, \dots, n\}$ and they do not already exist then create new nodes (in the connector graph) g_i, g_j with state label $\langle S_1, \dots, \bar{S}_i, \dots, S_h, S_{h+1}, \dots, \bar{S}_j, \dots, S_n \rangle$ and $\langle S_1, \dots, S'_i, \dots, S_h, S_{h+1}, \dots, S'_j, \dots, S_n \rangle$ respectively, where in AS_i $S_i \xrightarrow{t_i} S'_i$ and in AS_j $S_j \xrightarrow{v_j} S'_j$;
 - ii. if $j \in \{1, \dots, h\}$, $i \in \{h+1, \dots, n\}$ and they do not already exist then create new nodes (in the connector graph) g_i, g_j with state label $\langle S_1, \dots, \bar{S}_i, \dots, S_h, S_{h+1}, \dots, \bar{S}_j, \dots, S_n \rangle$ and $\langle S_1, \dots, S'_i, \dots, S_h, S_{h+1}, \dots, S'_j, \dots, S_n \rangle$ respectively, where in AS_i $S_i \xrightarrow{t_i} S'_i$ and in AS_j $S_j \xrightarrow{v_j} S'_j$;
 - iii. create the arc (g, t_i, g_i) in the connector graph;
 - iv. mark g_i as visited;
 - v. create the arc (g_i, \bar{v}_j, g_j) in the connector graph.
- (e) Perform recursively this procedure on all not marked (as visited) adjacent nodes of current node.

In Figure 6 we show the connector graph for the example illustrated in this section. The resulting CBA system is built as defined in Definition 2.

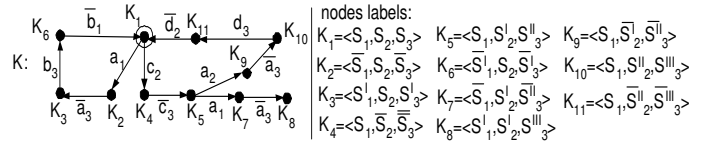


Figure 6: Connector graph of the example

In [15] we have proved that the CBA-system obtained by the connector synthesis process is equivalent to the corresponding CFA-system. To do this we have proved that the CFA-system can be simulated by the synthesized CBA-system (correctness of the synthesis) under a suitable notion of "state based" equivalence called CB-Simulation [15]. The starting point of CB-Simulation is the stuttering equivalence [20]. We have also proved that the connector does not introduce in the system any new logic (completeness of the synthesis).

3.2 Second step: Concurrency conflicts avoidance

The second step concerns the concurrency conflicts avoidance, which is performed on the CBA system. In [15], we have proved that if a concurrency conflict (i.e. coordination deadlock) is possible, then this results in a precise connector behavior that is detectable by observing the connector graph. To fix this problem it is enough to prune all the finite branches of the connector transition graph. The pruned connector preserves all the correct (with respect to deadlock freeness) behaviors of CFA-system [15]. In Figure 7 we show the concurrency conflict-free connector graph.

²By definition, both CFA and CBA systems exhibit only τ transitions.

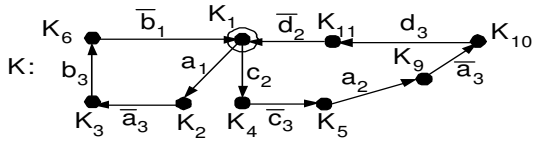


Figure 7: Deadlock-free connector graph of the example

3.3 Third step: Coordination policies enforcing

In this section we formalize the third step of the method of Figure 2. This step concerns the coordination policy enforcing on the connector graph.

3.4 Generic coordination policies specification

The coordination policies we want to enforce are related to behaviors of the CBA system. The ones that do not support the specified coordination policies represent policies-conflicting behaviors of the CBA system. Analogously to concurrency conflicts, we can solve conflicting behaviors of the CBA system that are identifiable with precise behaviors of the synthesized connector. A connector behavior is simply an execution path into connector graph. An execution path is a sequence of state's transition labels. Thus the coordination policies can be specified in terms of visible actions of each component on communication channel that connects the component to the connector: $AP = \{\alpha : \alpha = l_c \vee \alpha = \bar{l}_c \text{ with } l \in LA_{AC_i}, l \neq \tau, i = 1, \dots, n \text{ and } c \text{ is the identifier of the channel that connects } C_i \text{ to the connector}\}$.

By referring to the usual model checking approach [6] we specify every coordination policy through a temporal logic formalism. We choose *LTL* [6] (*Linear-time Temporal Logic*) as specification language. The above defined set AP is the set of atomic proposition on which we define the LTL formulas corresponding to the coordination policies. Refer to [6] for the standard LTL syntax and semantics.

3.5 Enforcing a coordination policy

The semantics of a LTL formula is defined with respect to a model represented by a Kripke structure [6]. We consider as Kripke structure corresponding to the connector graph K a connector model KS_K that represents the Kripke structure of K . KS_K is defined as follows:

Definition 7. Kripke structure of a connector graph K :

Let (N, LN, LA, A, k_1) be the connector graph K . We define the Kripke Structure of K , the Kripke structure $KS_K = (V, T, \{k_1\}, LV)$ where $V = N$, $T = A$, $LV = 2^{LA}$ with $LV(k_1) = \{\alpha_i : LA((\bar{k}, k_1)) = \alpha_i, (\bar{k}, k_1) \in A\}$. For each $v \in V$ then $LV(v)$ is interpreted as the set of atomic propositions true in state v .

In Figure 8, we show the Kripke structure of K . The node with an incoming little-arrow is the initial state k_1 .

Let P be the coordination policy specification (i.e. LTL formula), we can translate P in the corresponding Büchi Automaton [6, 10] B_P :

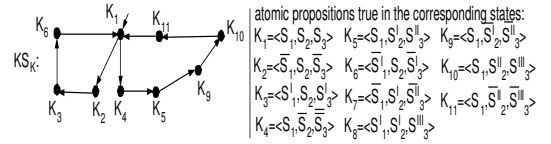


Figure 8: Kripke structure of K

Definition 8. Büchi Automaton:

A Büchi Automaton B is a 5-tuple $\langle S, A, \Delta, q_0, F \rangle$, where S is a finite set of states, A is a set of actions, $\Delta \subseteq S \times A \times S$ is a set of transitions, $q_0 \in S$ is the initial state, and $F \subseteq S$ is a set of accepting states. An *execution* of B on an infinite word $w = a_0 a_1 \dots$ over A is an infinite sequence $\sigma = q_0 q_1 \dots$ of elements of S , where $(q_i, a_i, q_{i+1}) \in \Delta, \forall i \geq 0$. An execution of B is *accepting* if it contains some accepting state of B an infinite number of times. B accepts a word w if there exists an accepting execution of B on w .

Referring to our example we consider the following behavioral property: $P = G(F(a_1)) \wedge G(F(a_2))$; this property is the specification of all CFA system behaviors that guarantee the evolution of all components in the system. The synthesized connector avoids starvation by satisfying this property. Figure 9 we show B_P . p_0 and p_2 are the initial and accepting state respectively.

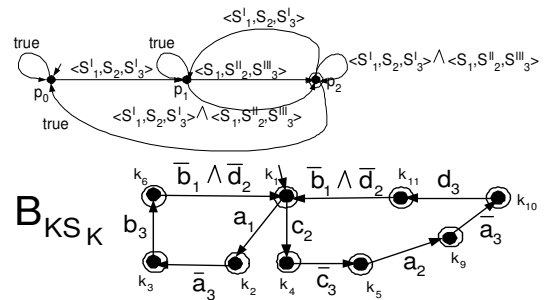


Figure 9: Büchi Automata B_P and B_{KS_K} of P and KS_K respectively

Given a Büchi Automaton A , $L(A)$ is the *language* consisting of all words accepted by A . Moreover to a Kripke structure T corresponds a Büchi Automaton B_T [6]. We can derive B_{KS_K} as the Büchi Automaton corresponding to KS_K (see Figure 9). The double-circled states are accepting states. Thus given $B_{KS_K} = (N, \Delta, \{s\}, N)$ and $B_P = (S, \Gamma, \{v\}, F)$ the method performs the following enforcing procedure in order to synthesize a deadlock-free coordinator graph that supports P :

1. build the automaton that accepts $L(B_{KS_K}) \cap L(B_P)$; this automaton is defined as $B_{intersection}^{K,P} = (S \times N, \Delta', \{v, s\}, F \times N)$ where $(\langle r_i, q_j \rangle, a, \langle r_m, q_n \rangle) \in \Delta'$ if and only if $(r_i, a, r_m) \in \Gamma$ and $(q_j, a, q_n) \in \Delta$;
2. if $B_{intersection}^{K,P}$ is not empty return $B_{intersection}^{K,P}$ as the Büchi Automaton corresponding to the P -satisfying execution paths of K .

In Figure 10, we show $B_{intersection}^{K,P}$.

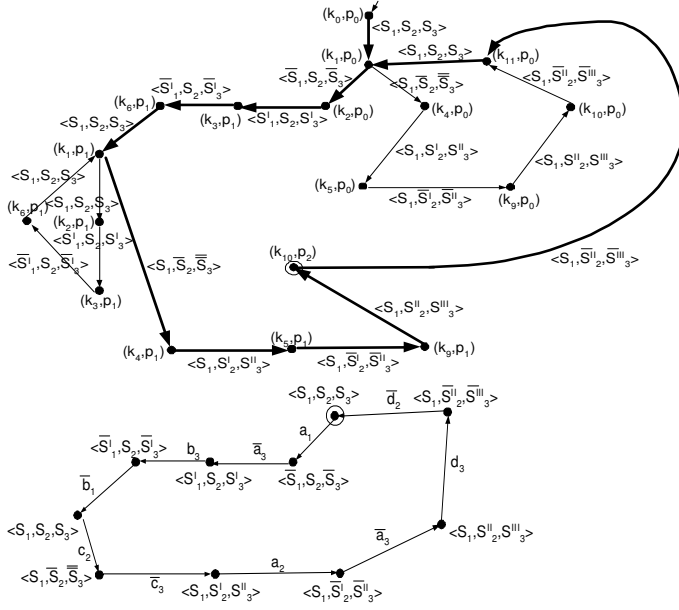


Figure 10: $B_{intersection}^{K,P}$ and conflict-free coordination policy-satisfying connector graph of the explanatory example

Finally our method derives from $B_{intersection}^{K,P}$ the corresponding connector graph. This graph is constructed by considering the only execution paths of $B_{intersection}^{K,P}$ that contain only *accepting cycles* (see the path made of bold arrows in Figure 10); we define an *accepting cycle* of $B_{intersection}^{K,P}$ as follow:

Definition 9. Accepting cycle of $B_{intersection}^{K,P}$:

Let $B_{intersection}^{K,P} = (S \times N, \Delta', \{<v, s>\}, F \times N)$ be the automaton that accepts $L(B_{KS_K}) \cap L(B_P)$. We define accepting cycle of $B_{intersection}^{K,P}$ a sequence of states $\gamma = s_1, s_2, \dots, s_n$ such that $\forall i = 1, \dots, n : s_i \in S \times N$; for $1 \leq i \leq n-1, (s_i, s_{i+1}) \in \Delta'$ and $(s_n, s_1) \in \Delta'$; and $\exists k = 1, \dots, n : k \in F \times N$.

Then, to terminate the construction of the P-satisfying connector graph, the method prunes the possible branches terminating with stop nodes. In Figure 10, we show the conflict-free coordination policy-satisfying connector graph for our explanatory example. By visiting this graph and by exploiting the information stored in its states and transitions we can derive the code that implements the P-satisfying deadlock-free connector (i.e. the coordinator) analogously to what done for deadlock-free connectors [14]. In the following we show the conflict-free policy-satisfying code implementing the methods *a* and *c* of the connector component *K*. The implementation refers to Microsoft COM (*Component Object Model*) components and uses C++ with ATL (*Active Template Library*) as programming environment. *c3Obj* is an instance of the inner COM server corresponding to C_3 and encapsulated into connector component *K*.

```

HRESULT a(/* params list of a */) {
    if(sLbl == 1) {
        if((chId == 1) && (pState == 0)) {
            return c3Obj->a(/* params list of a */);
            pState = 1; sLbl = 1;
        }
    }
    else if(sLbl == 5) {
        if((chId == 2) && (pState == 1)) {
            return c3Obj->a(/* params list of a */);
            pState = 0; sLbl = 10;
        }
    }
    return E_HANDLE;
}

HRESULT c(/* params list of c */) {
    if(sLbl == 1) {
        if((chId == 2) && (pState == 1)) {
            return c3Obj->c(/* params list of c */);
            pState = 1; sLbl = 5;
        }
    }
    return E_HANDLE;
}

```

The connector component *K* implements the COM interface *IC3* of the component C_3 by defining a COM class *K* and by implementing a wrapping mechanism in order to wrap the requests that C_1 and C_2 perform on component C_3 . In the following we show fragments of the IDL (*Interface Definition Language*) definition for *K*, of the *K* COM library and of the *K* COM class respectively.

```

import ic3.idl; ... library K_Lib {
    ...
    coclass K {
        [default] interface IC3;
    }
}

...

class K : public IC3 {
    // stores the current state of the connector
    private static int sLbl;

    // stores the current state of the
    // property automaton
    private static int pState;

    // stores the number of clients
    private static int clientsCounter = 0;

    // channel's number of a client
    private int chId;

    // COM smart pointer; is a reference to
    // the C3 server object
    private static C3* c3Obj;

    ...

    // the constructor
    K() {
        sLbl = 1;
        pState = 0;
        clientsCounter++;
        chId = clientsCounter;
        c3Obj = new C3();
        ...
    }

    // implemented methods
    ...
}

```

In [18] we prove the correctness of the property enforcing procedure. We prove that the CBA-system based on the property-satisfying deadlock-free connector preserves all the property-satisfying behaviors of the corresponding deadlock-free CFA-system.

4. RELATED WORKS

The architectural approach to correct and automatic connector synthesis presented in this paper is related to a large number of other problems that have been considered by researchers over the past two decades. For the sake of brevity

we mention below only the works closest to our approach. The most strictly related approaches are in the "scheduler synthesis" research area. In the discrete event domain they appear as "supervisory control" problem [3, 22, 5, 24, 25]. In very general terms, these works can be seen as an instance of a problem similar to the problem treated in our approach. However the application domain of these approaches is sensibly different from the software component domain. Dealing with software components introduces a number of problematic dimensions to the original synthesis problem. There are two main problems with this approach: i) the computational complexity and the state-space explosion and ii) in general the approach is not compositional. The first problem can be avoided by using a logical encoding of the system specification in order to use a more efficient data structure (i. e. BDD (Binary Decision Diagram)) to perform the supervisor synthesis; however the second problem cannot be avoided and only under particular conditions it is possible to synthesize the global complete supervisor by composing modular supervisors. While the state-space explosion is a problem also present in our approach, on the other side we have proved in [15] that our approach is always compositional. It means that if we build the connector for a given set of components and later we add a new component in the resulting system we can extend the already available connector and we must not perform again the entire synthesis process.

Other works that are related to our approach, appear in the *model checking of software components* context in which CRA (*Compositional Reachability Analysis*) techniques are largely used [12, 11]. Also these works can be seen as an instance of the general problem formulated in Section 3. They provide an optimistic approach to software components model checking. These approaches suffer the state-space explosion problem. However this problem is raised only in the worst case that may not be the case often in practice. In these approaches the assumptions that represent the *weakest* environment in which the components satisfy the specified properties are automatically synthesized. However the synthesized environment does not provide a model for the properties satisfying glue code. The synthesized environment may be rather used for runtime monitoring or for components retrieval.

Recently promising formal techniques for the compositional analysis of component based design have been developed [7, 8]. The key of these works is the modular-based reasoning that provides a support for the modular checking of behavioral properties. The goal of these works is quite different from our in fact they are related only to software components interfaces compatibility check. Thus they provide only a check on component-based design level.

5. CONCLUSION AND FUTURE WORKS

In this paper we have described a connector-based architectural approach to component assembly. Our approach focusses on detection and recovery of the assembly behavioral failures. A key role is played by the software architecture structure since it allows all the interactions among components to be explicitly routed through a synthesized connector. We have applied our approach to an example and we have discussed its implications on the actual nature

of black-box components. As far as components are concerned we only assumed to have a CCS description of the components behavior. For the purpose of this paper this is an acceptable assumption. However our framework allows to automatically derive these CCS descriptions from specifications that are common practice in real-scale contexts. For behavioral properties we have shown in this paper how to go beyond deadlock. The complexity of the synthesis and analysis algorithm is exponential either in space and time. This value of complexity is obtained by considering the unification process complexity and the size of the data structure used to build the connector graph. At present we are studying better data structures for the connector model in order to reduce their size. By referring to the automata based model checking [6], we are also working to perform on the fly analysis during the connector model building process. Other possible limits of the approach are: i) we completely centralize the connector logic and we provide a strategy for the connector source code derivation step that derives a centralized implementation of the connector component. We do not think this is a real limit because even if we centralize the connector logic we can actually think of deriving a distributed implementation of the connector component; ii) we assume that an HMSC and bMSC specification for the system to be assembled is provided. Although this is reasonable to be expected, it is interesting to investigate testing and inspection techniques to directly derive from a COTS (black-box) component some kind (possibly partial) behavioral specification; iii) we assume also an LTL specification for the behavioral property to be checked. It is interesting to find a more user-friendly property specification; for example by extending the HMSC and bMSC notations to express more complex system's components interaction behaviors.

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6. REFERENCES

- [1] Itu telecommunication standardisation sector, itu-t recommendation z.120. message sequence charts. (msc'96). Geneva 1996.
- [2] R. Allen and D. Garlan. A formal basis for architectural connection. *ACM Transactions On Software Engineering and Methodology*, Vol. 6, No. 3, pp. 213-249, 6(3):213-249, July 1997.
- [3] S. Balemi, G. J. Hoffmann, P. Gyugyi, H. Wong-Toi, and G. F. Franklin. Supervisory control of a rapid thermal multiprocessor. *IEEE Transactions on Automatic Control*, 38(7):1040-1059, July 1993.
- [4] L. Bass, P. Clements, and R. Kazman. *Software Architecture in Practice*. Addison Wesley, 1998.
- [5] B. A. Brandin and W. M. Wonham. Supervisory control of timed discrete-event systems. *IEEE Transactions on Automatic Control*, 39(2), February 1994.
- [6] E. M. Clarke, O. Grumberg, and D. A. Peled. *Model Checking*. The MIT Press, Cambridge, Massachusetts, London, England, 2001.

- [7] L. de Alfaro and T. Heininger. Interface automata. In *ACM Proc. of the joint 8th ESEC and 9th FSE*, ACM Press, Sep 2001.
- [8] L. de Alfaro and T. Heininger. Interface theories for component-based design. In *In Proc. of EMSOFT'01: Embedded Software, LNCS 2211*, pp. 148-165. Springer-Verlang, 2001.
- [9] D. Garlan and D. E. Perry. *Introduction to the Special Issue on Software Architecture, Vol. 21. Num. 4.* pp. 269-274, April 1995.
- [10] R. Gerth, D. Peled, M. Y. Vardi, and P. Wolper. Simple on-the-fly automatic verification of linear temporal logic. in *Proc. of the 15th IFIP/WG6.1 Symposium on Protocol Specification, Testing and Verification (PSTV'95)*, June 1995.
- [11] D. Giannakopoulou, J. Kramer, and S. Cheung. Behaviour analysis of distributed systems using the tracta approach. *Journal of Automated Software Engineering, special issue on Automated Analysis of Software*, 6(1):7-35, January 1999.
- [12] D. Giannakopoulou, C. S. Pasareanu, and H. Barringer. Assumption generation for software component verification. *Proc. 17th IEEE Int. Conf. Automated Software Engineering 2002*, September 2002.
- [13] P. Inverardi and M. Tivoli. Deadlock-free software architectures for com/dcom applications. *Journal of Systems and Software, Volume 65, Issue 3, 15 March 2003, Pages 173-183, Component-Based Software Engineering*.
- [14] P. Inverardi and M. Tivoli. Automatic synthesis of deadlock free connectors for com/dcom applications. In *ACM Proceedings of the joint 8th ESEC and 9th FSE*, ACM Press, Vienna, Sep 2001.
- [15] P. Inverardi and M. Tivoli. Connectors synthesis for failures-free component based architectures. *Technical Report, University of L'Aquila, Department of Computer Science*, http://sahara.di.univaq.it/tech.php?id_tech=7 or <http://www.di.univaq.it/~tivoli/ffsynthesis.pdf>, ITALY, January 2003.
- [16] P. Inverardi, M. Tivoli, and A. Bucchiarone. Automatic synthesis of coordinators of cots group-ware applications: an example. *International Workshop on Distributed and Mobile Collaboration (DMC 2003)*, <http://www.di.univaq.it/tivoli/Publications/Full/DMC2003.pdf>, 9-11 June, Linz, Austria WETICE 2003.
- [17] P. Inverardi, M. Tivoli, and A. Bucchiarone. Coordinators synthesis for cots group-ware systems: an example. *Technical Report, University of L'Aquila, Department of Computer Science*, <http://www.di.univaq.it/tivoli/cscw-techrep.pdf>, ITALY, March 2003.
- [18] P. Inverardi, M. Tivoli, and A. Bucchiarone. Failures-free connector synthesis for correct components assembly. *Technical Report, University of L'Aquila, Department of Computer Science*, http://www.di.univaq.it/tivoli/ffs_techrep.pdf, ITALY, March 2003.
- [19] R. Milner. *Communication and Concurrency*. Prentice Hall, New York, 1989.
- [20] R. D. Nicola and F. Vaandrager. Three logics for branching bisimulation. *Journal of the ACM*, 42(2):458-487, 1995.
- [21] P. Inverardi and M. Tivoli. Automatic failures-free connector synthesis: An example. *Technical Report, published on the Monterey 2002 Workshop Proceedings: Radical Innovations of Software and Systems Engineering in the Future, Universita' Ca' Foscari di Venezia, Dip. di Informatica, Technical Report CS-2002-10*, September 2002.
- [22] P. J. Ramadge and W. M. Wonham. Supervisory control of a class of discrete event processes. *Siam J. Control and Optimization*, 25(1), January 1987.
- [23] C. Szyperski. *Component Software. Beyond Object Oriented Programming*. Addison Wesley, Harlow, England, 1998.
- [24] E. Tronci. On computing optimal controllers for finite state systems. *Proc. of 35th IEEE Conf. on Decision and Control*, 1996.
- [25] E. Tronci. Automatic synthesis of controllers from formal specifications. *Proc. of 2nd IEEE Int. Conf. on Formal Engineering Methods*, December 1998.
- [26] S. Uchitel, J. Kramer, and J. Magee. Detecting implied scenarios in message sequence chart specifications. In *ACM Proceedings of the joint 8th ESEC and 9th FSE*, Vienna, Sep 2001.