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741 OP-AMP

Generally, operational amplifiers are extremely high voltage gain op-amps and they are standard building blocks of analogue circuits. The most commonly used op-amp is IC741. The 741 op-amp is a voltage amplifier, it inverts the input voltage at the output, can be found almost everywhere in electronic circuits.

Let's see the pin configuration and testing of 741 op-amps. Usually, this is a numbered counter clockwise around the chip. It is an 8 pin IC. They provide superior performance in integrator, summing amplifier and general feedback applications. These are high gain op-amp; the voltage on the inverting input can be maintained almost equal to Vin.

It is a 8-pin dual-in-line package with a pinout shown above.

Pin 1: Offset null.

Pin 2: Inverting input terminal.

Pin 3: Non-inverting input terminal.

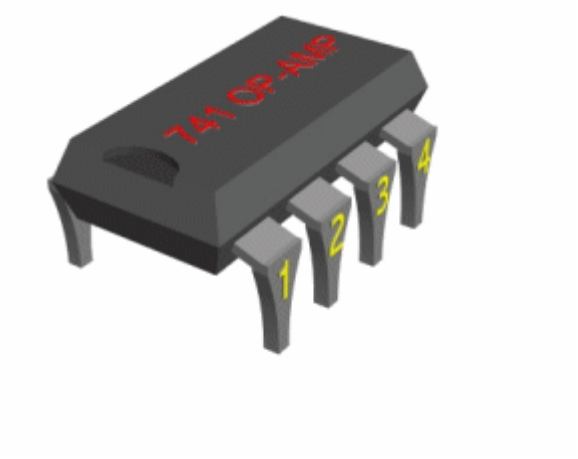
Pin 4: –VCC (negative voltage supply).

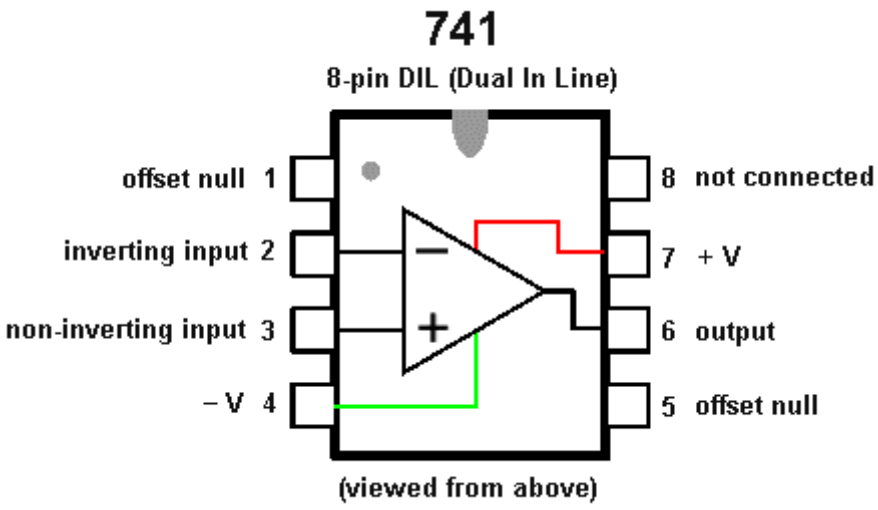
Pin 5: Offset null.

Pin 6: Output voltage.

Pin 7: +VCC (positive voltage supply).

Pin 8: No Connection.





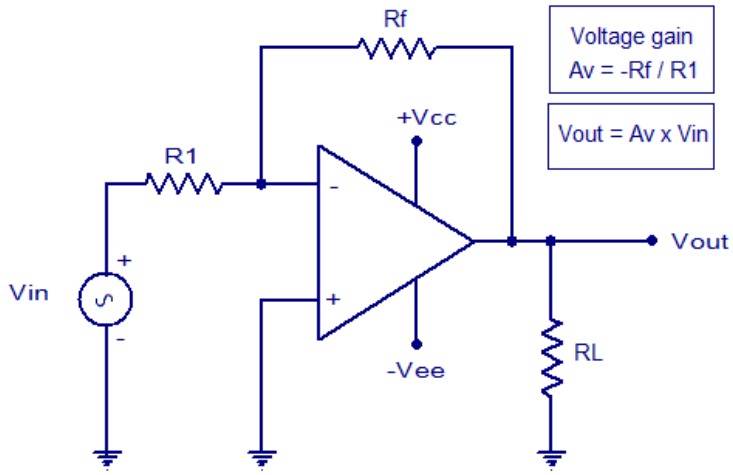
Experiment No: 1

AIM: Design and realize Inverting and Non-inverting amplifier using 741 Op-amp.

Apparatus Required: CRO, Function Generator, Bread Board, 741 IC, ±12V supply, Resistors 1KΩ, 10KΩ, and Connecting leads.

Theory:

An inverting amplifier using opamp is a type of amplifier using opamp where the output waveform will be phase opposite to the input waveform. The input waveform will be amplifier by the factor Av (voltage gain of the amplifier) in magnitude and its phase will be inverted. In the inverting amplifier circuit the signal to be amplified is applied to the inverting input of the opamp through the input resistance R1. Rf is the feedback resistor. Rf and Rin together determine the gain of the amplifier. Inverting operational amplifier gain can be expressed using the equation Av = – Rf/R1. Negative sign implies that the output signal is negated. The circuit diagram of a basic inverting amplifier using opamp is shown below.



opamp inverting amplifier

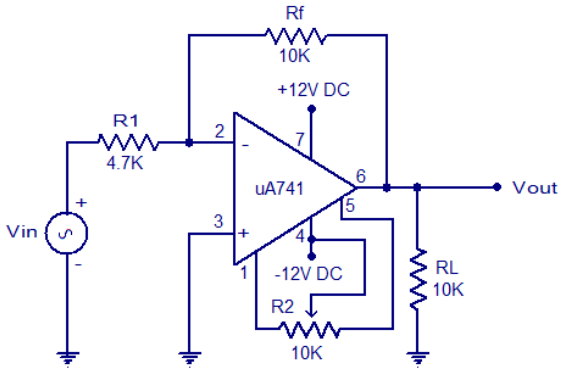
The input and output waveforms of an inverting amplifier using opamp is shown below. The graph is drawn assuming that the gain (Av) of the amplifier is 2 and the input signal is a sine wave. It is clear from the graph that the output is twice in magnitude when compared to the input (Vout = Av x Vin) and phase opposite to the input.

Practical inverting amplifier using 741.

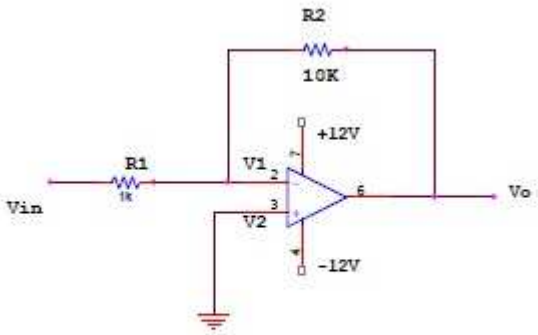
A simple practical inverting amplifier using 741 IC is shown below. uA 741 is a high performance and of course the most popular operational amplifier. It can be used in a verity of applications like integrator, differentiator, voltage follower, amplifier etc. uA 741 has a wide supply voltage range (+/-22V DC) and has a high open loop gain. The IC has an integrated compensation network for improving stability and has short circuit protection.

Signal to be amplified is applied to the inverting pi (pin2) of the IC. Non inverting pin (pin3) is connected to ground. R1 is the input resistor and Rf is the feedback resistor. Rf and R1 together sets the gain of the amplifier. With the used values of R1 and Rf the gain will be 10

(Av = -Rf/R1 = 10K/1K = 10). RL is the load resistor and the amplified signal will be available across it. POT R2 can be used for nullifying the output offset voltage. If you are planning to assemble the circuit, the power supply must be well regulated and filtered. Noise from the power supply can adversely affect the performance of the circuit. When assembling on PCB it is recommended to mount the IC on the board using an IC base.



opamp inverting amplifier



INVERTING AMPLIFIER

In the inverting amplifier only one input is applied and that is to the inverting input (V2) terminal. The Non inverting input terminal (V1) is grounded.

Since, V1=0 V& V2=Vin

Vo= -A Vin

The negative sign indicates the output voltage is 180^0 out of phase with respect to the input and amplified by gain A.

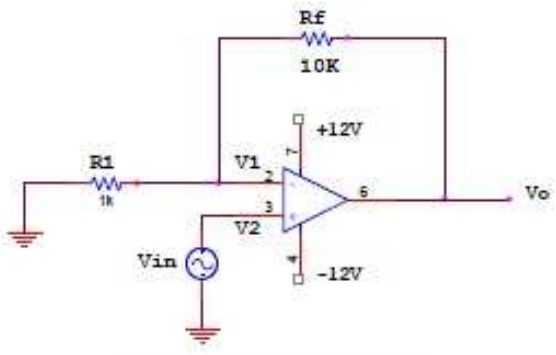
Practical Non-inverting amplifier using 741:

The input is applied to the non-inverting input terminal and the Inverting terminal is connected to the ground.

V1= Vin & V2=0 Volts

Vo= A Vin

The output voltage is larger than the input voltage by gain A & is in phase with the input signal.

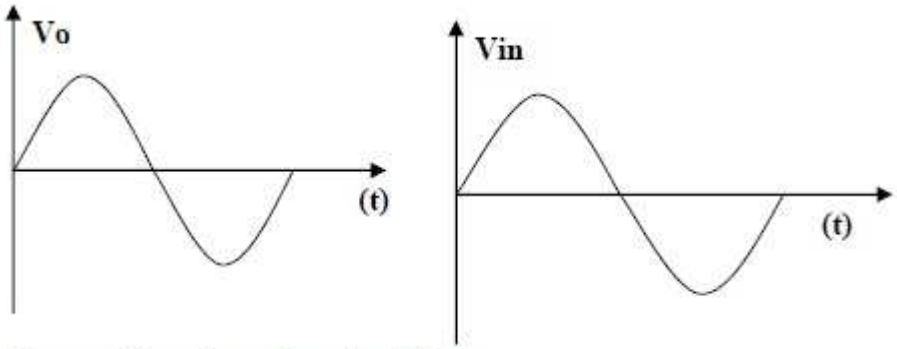


NON-INVERTING AMPLIFIER

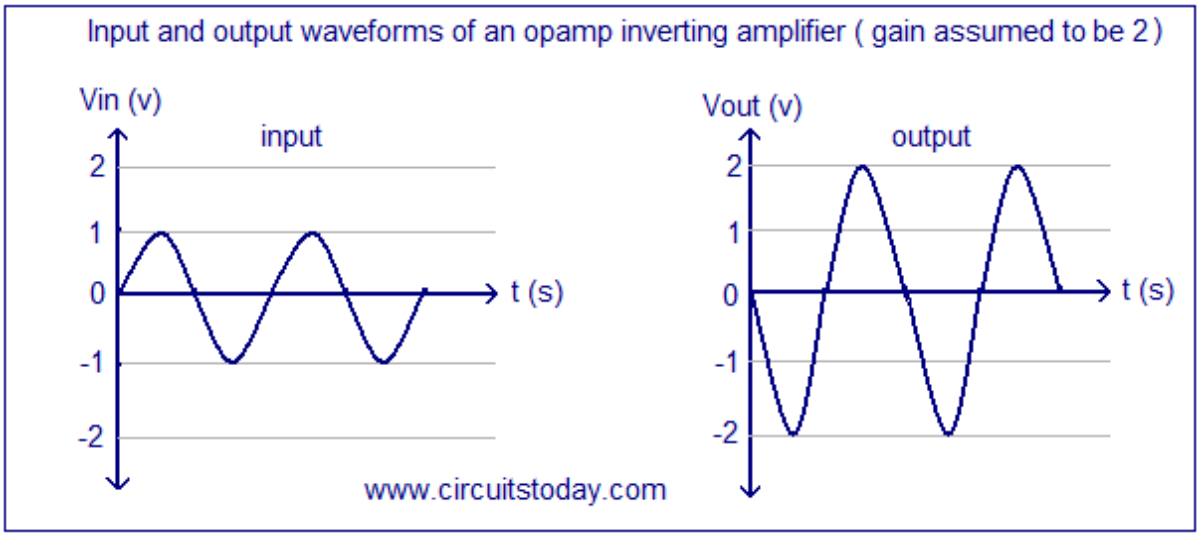
Procedure:

1) Connect the circuit for inverting, non inverting amplifier on a breadboard.
2) Connect the input terminal of the op-amp to function generator and output terminal to CRO.
3) Feed input from function generator and observe the output on CRO.
4) Draw the input and output waveforms on graph paper.

Output Waveform:



Output: Non- Inverting Amplifier



Experiment No: 2

AIM: Design and realize voltage follower and differential amplifier using 741 Op-amp.

Apparatus Required: CRO, Function Generator, Bread Board, 741 IC, ±12V supply, Resistors, and Connecting leads.

Theory:

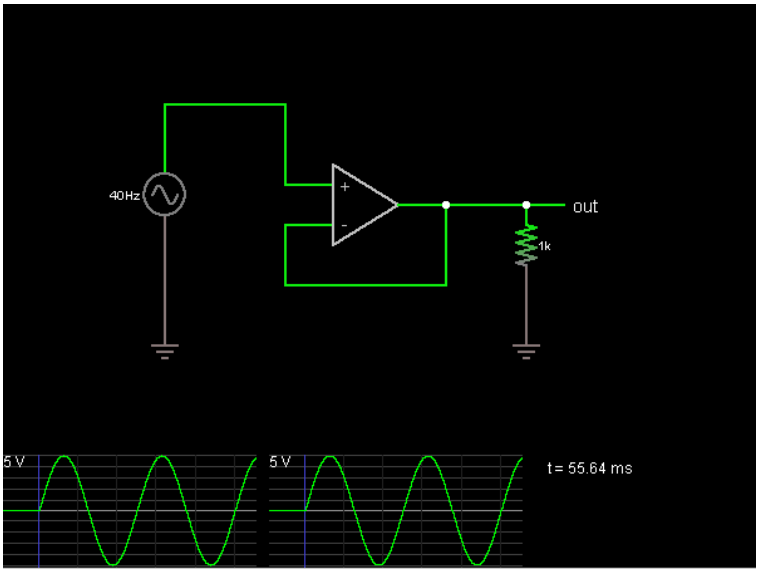
Voltage follower:

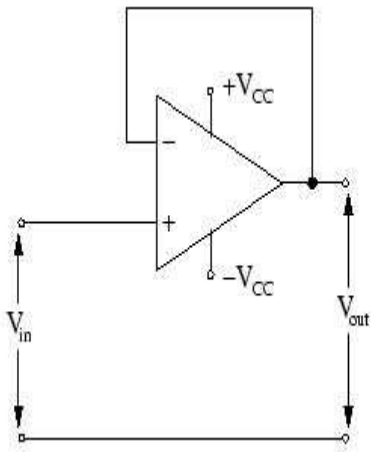
This is a voltage follower or buffer amplifier circuit, where the output is simply equal to the input. The advantage of this circuit is that the op-amp can provide current and power gain; the op-amp draws almost no current from the input. It provides low output impedance to any circuit using the output of the follower, meaning that the output will not drop under load. The load is a 1k resistor in this case; the op-amp provides all the current needed to drive the load, without requiring any current from the input.

1) Rf = 0, therefore no amplification. Gain = 1 + (Rf/Rin)

2) Output voltage is equal to input voltage.

3) Use to buffer/isolate circuit. Voltage is the same, but current is supplied by Vss rather than Vin





Differential Amplifier:

This circuit outputs the difference in voltage between two input signals. In this case, the first input is a 60 Hz signal, and the second input is a 60 Hz signal with 120 Hz square wave added in. (In this simulation, the two signals are added simply by connecting the two sources in series, which is convenient but not realistic.)

The second input signal is driving two resistors, which act as a voltage divider, and the + input of the op-amp is connected between them, where the voltage is equal to half the second

input signal. The op-amp attempts to keep its – input at the same voltage as the + input. The two resistors on top act as a voltage divider, making the – input halfway between the first input signal and the op-amp output.

If $V_+ = 1/2\ In_2 = V_- = 1/2\ (In_1 + output)$, then the output = $In_2 - In_1$, or the difference between the two inputs.

Referring to the above circuit, we understand that the differential amplifier is a combination of inverting and non-inverting amplifiers. That is, when v_x is reduced to zero the circuit is a non-inverting amplifier, whereas the circuit is an inverting amplifier when input v_y is reduced to zero.

The circuit above has two inputs, v_x and v_y ; we will, therefore, use the super position theorem in order to establish the relationship between input and output. When $v_y = 0V$, the configuration becomes an inverting amplifier; hence the output due to v_x only is :

$v_{ox} = - \{ R_F(v_x) / R_1 \}$……..(a)

Similarly, when $v_x = 0V$, the configuration is a non inverting amplifier having a voltage divider network composed of R_2 and R_3 at the non inverting input.

Therefore :

$v_1 = \{ R_3 (v_y) / (R_2+R_3) \}$

and the output due to v_y then is

$v_{oy} = \{ 1 + (R_F / R_1) \} * v_1$

that is,

$v_{oy} = \{R_3 / (R_1+R_3)\}* \{(R_1+R_F) / R_1\}* v_y$

Since, $R_1 = R_2$ and $R_F = R_3$,

$v_{oy} = R_F (v_y) / R_1$……(b)

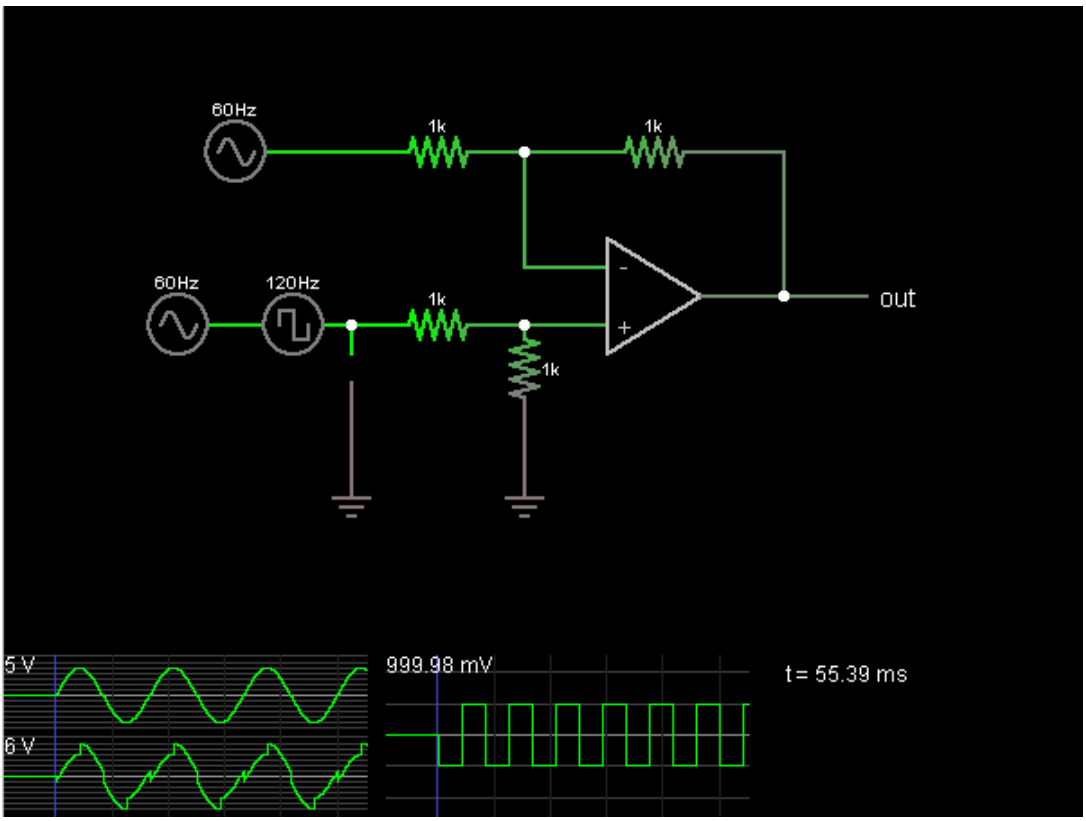
Thus, from equations (a) and (b), the net output voltage is :

$v_o = v_{ox} + v_{oy}$

or, $v_o = - \{(R_F / R_1) (v_x – v_y)\} = - \{ R_F(v_y) / R_1 \}$

or, the differential voltage gain,

$$\boxed{A_D = v_o / v_y = - \{ R_F / R_1 \}}$$

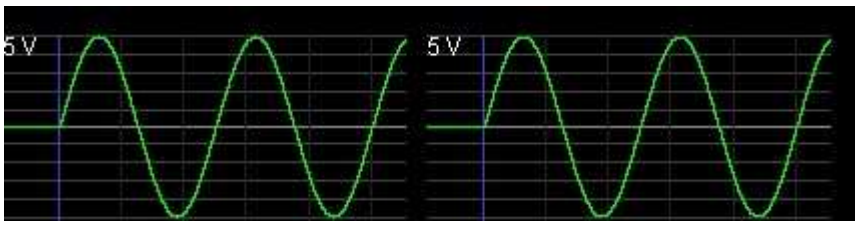


Procedure:

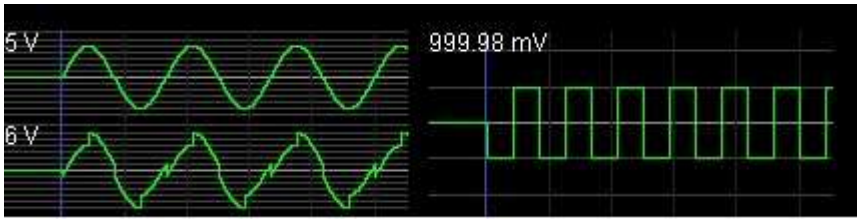
1) Connect the circuit as per the circuit diagram.
2) Apply the input voltages (vx and v_y) to the input terminals.
3) Check the output ie, $v_x - v_y$.
4) Note that the output will be N times more than the differential input because we have set gain equal to N (where N can be any number depending upon the value of R_F and R_1).
5) Take the various values of v_x and v_y and measure the output.

Output Waveform:

Voltage follower outputs waveforms:



Differential amplifier output waveforms:



Experiment No: 3

AIM: Design and verify the operations of op amp adder (summing) and subtractor circuit using 741 Op-amp.

Apparatus Required: CRO, Function Generator, Bread Board, 741 IC, ±12V supply, Resistors, and Connecting leads.

Theory:

Adder (Summing Amplifier):

Op-amp may be used to perform summing operation of several input signals in inverting in inverting and non-inverting mode. The input signals to be summed up are given to inverting terminal or non-inverting terminal through the input resistance to perform inverting and non-inverting summing operations respectively.

If the input to the inverting amplifier is increased, the resulting circuit is known as adder. Output is a linear summation of number of input signals. Each input signal produces a component of the output signal that is completely independent of the other input signal. When there are two inputs i.e.

$$Vo = -(V1+V2)$$

This is the inverted algebraic sum of all the inputs. If we connect the inputs to non inverting terminal then the adder is non inverting adder.

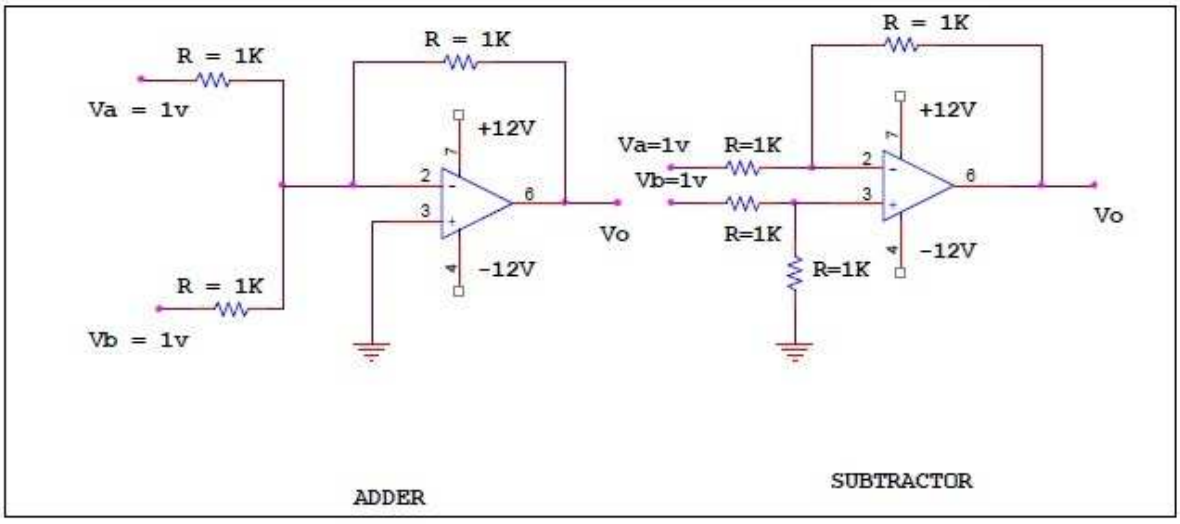
Subtractor: The basic difference amplifier can be used as a subtractor. The signals to be subtracted are connected to opposite polarity inputs i.e. in inverting or non-inverting terminals of the op-amp.

A circuit that finds the difference between two signals is called a subtractor. The two inputs are applied at the inverting & non inverting terminal of op-amp. If all external resistance are equal in value, so the gain of the amplifier is equal to 1. The output voltages of the differential amplifier with a gain of unity is,

$$Vo = -(R/R\ (Va-Vb)$$

$$Vo = -(Va-Vb)$$

Circuit Diagram:



S.No.	V1	V2	Theoretical V0=V1+V2	Practical V0
1.	5	3.4	8.4	8.5
2.	10	10	20	21.8

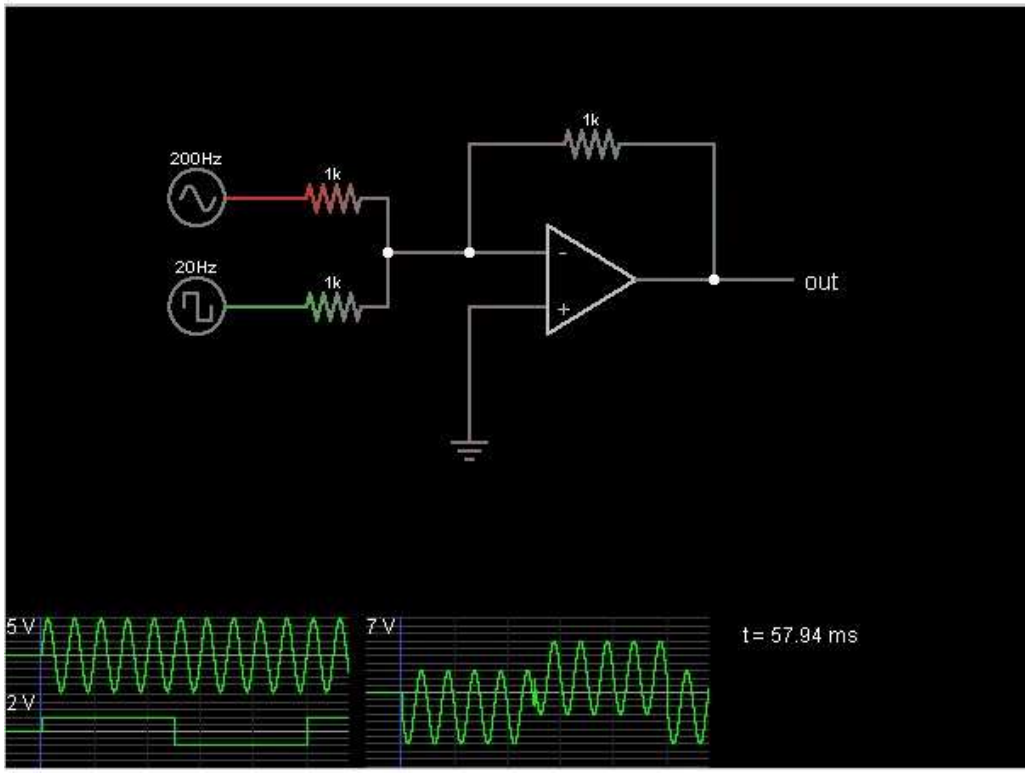
Summing Amplifier

S.No.	V1	V2	Theoretical V0=V1-V2	Practical V0
1.	10	7	3	3.003
2.	10	12	-2	-2.01

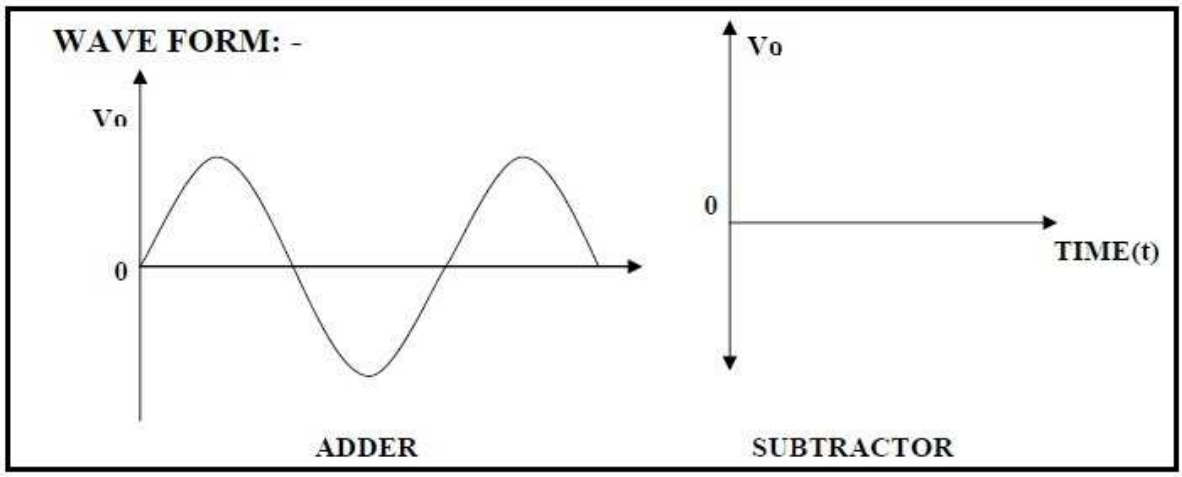
Subtractor

Procedure:

1) Apply two different sine waves signal to the input of the adder and subtractor.
2) Give the input amplitude of 5v peak to peak and frequency of 1 kHz.
3) Verify the output on CRO.
4)



Waveforms:



Result: Output is a true replica of the subtraction values of the two inputs and addition of two input values.

Experiment No: 4

AIM: Verify the operation of a differentiator circuit using op amp 741.

Apparatus Required: CRO, Function Generator, Bread Board, and 741 IC, ±12V supply, Resistors, Capacitors and Connecting leads.

Theory:

Differentiator circuits as its name implies, performs the mathematical operation of differentiator, that is, the output waveform is the derivative of the input. The differentiator may be constructed from a basic inverting amplifier when an input resistor R1 is replaced by a capacitor C,

$$Vo = -Rf\ C\ d\ Vin\ /dt$$

Thus, the output Vo is equal to the Rf C times the negative instantaneous rate of change of the input voltage Vin with time.

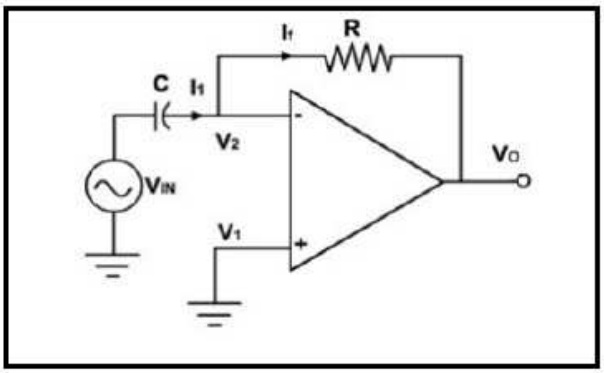
The right-hand side of the capacitor is held to a voltage of 0 volts, due to the "virtual ground" effect. Therefore, current "through" the capacitor is solely due to *change* in the input voltage. A steady input voltage won't cause a current through C, but a *changing* input voltage will.

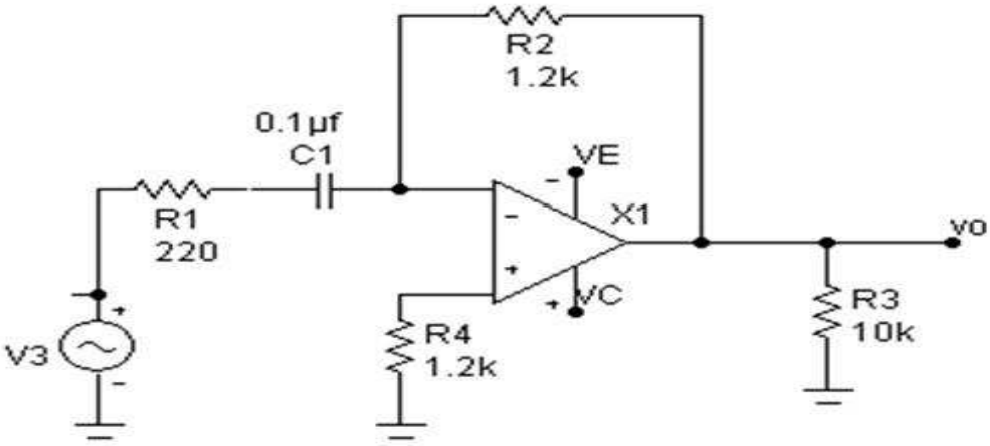
Capacitor current moves through the feedback resistor, producing a drop across it, which is the same as the output voltage. A linear, positive rate of input voltage change will result in a steady negative voltage at the output of the op-amp. Conversely, a linear, negative rate of input voltage change will result in a steady positive voltage at the output of the op-amp. This polarity inversion from input to output is due to the fact that the input signal is being sent (essentially) to the inverting input of the op-amp, so it acts like the inverting amplifier mentioned previously. The faster the rate of voltage change at the input (either positive or negative), the greater the voltage at the output.

The formula for determining voltage output for the differentiator is as follows:

$$V_{out} = -RC\ \frac{dv_{in}}{dt}$$

Circuit Diagram:





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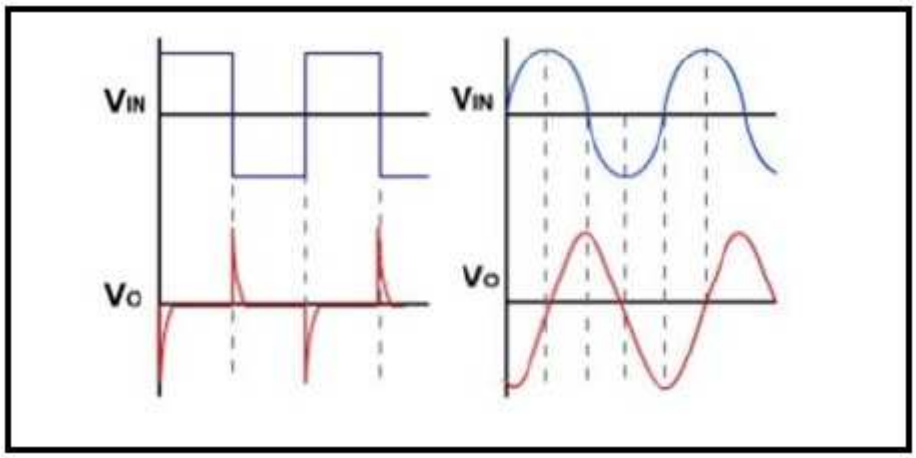
Procedure:

1) Connect the circuit as per the circuit diagram.
2) Apply the input signals i.e, Sinusoidal, Square waves.
3) Check the output waveform i.e, the wave shape of the signal.
4) Note that the output will be the differentiation of the applied signal or not.
5) Plot various input output wave shapes.

Observation table:

Sr.No.	I/P Voltage Vin	O/P Voltage Vo	Frequency in KHz.	Gain=20log Vo/Vin

Graph:



Result: Wave forms shows differentiator is a high pass filter.

Experiment No: 5

AIM: Verify the operation of a integrator circuit using op amp 741 and show that it acts as a low pass filter.

Apparatus Required: CRO, Function Generator, Bread Board, and 741 IC, ±12V supply, Resistors10KΩ, 1KΩ, Capacitors0.1µf and Connecting leads.

Theory:

A circuit in which the output waveform is the integral of the input wave is the integrator. Such a circuit is obtained by using a basic inverting amplifier configuration. If the feedback resistor Rf is replaced by a capacitor C. The output voltage can be obtained by,

$$Vo = -1/RCf \int Vin\, dt + C$$

Where C is the integration constant and proportional to the value of the output voltage Vo at time t=0 sec. Thus, the output voltage is directly proportional to the negative integral of the input voltage and inversely proportional to the time constant R Cf. The convenient way to introduce the AC integration circuit is through frequency response and impedance consideration. The transfer function for the true integrator is given by,

$$H(j\omega) = -Zf / Zi = -\frac{1/j\omega c}{R}$$

$$H(j\omega) = -1/j\omega cR$$

Amplitude response, M(w)=1/wRC It is clear that integration is a form of low pass filtering i.e., the function is very large at low frequency and decreases as the frequency increases.

The circuit operates by passing a current that charges or discharges the capacitor over time. If the op-amp is assumed ideal, nodes *v1* and *v2* are held equal, and so *v2* is a virtual ground. The input voltage passes a current $\frac{v_{in}}{R_1}$ through the resistor and series capacitor, which charges or discharges the capacitor over time. Because the resistor and capacitor are connected to a virtual ground, the input current does not vary with capacitor charge and a linear integration operation is achieved.

The circuit can be analyzed by applying kirchhoff's current law at the node *v2*, keeping ideal op-amp behaviour in mind.

$$i_1 = I_B + i_F$$

$I_B = 0$ in an ideal op-amp, so:

$$i_1 = i_F$$

Furthermore, the capacitor has a voltage-current relationship governed by the equation:

$$I_C = C\frac{dV_c}{dt}$$

Substituting the appropriate variables:

$$\frac{v_{in} - v_2}{R_1} = C_F\frac{d(v_2 - v_o)}{dt}$$

$v_2 = v_1 = 0$ in an ideal op-amp, resulting in:

$$\frac{v_{in}}{R_1} = -C_F\frac{dv_o}{dt}$$

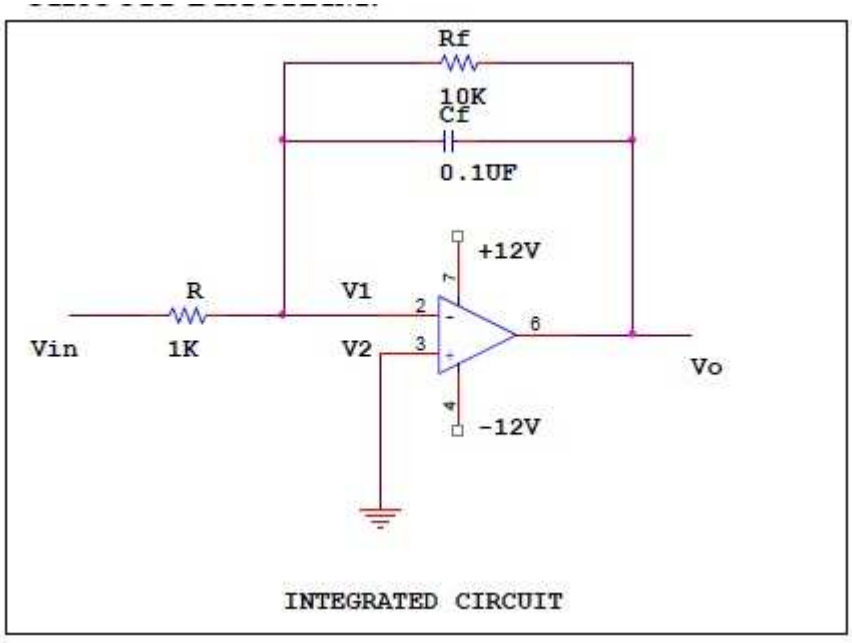
Integrating both sides with respect to time:

$$\int_0^t \frac{v_{in}}{R_1}\,dt = -\int_0^t C_F\frac{dv_o}{dt}\,dt$$

If the initial value of *vo* is assumed to be 0 V, this results in a DC error of:[1]

$$v_o = -\frac{1}{R_1 C_F}\int_0^t v_{in}\,dt$$

Circuit Diagram:



Procedure:

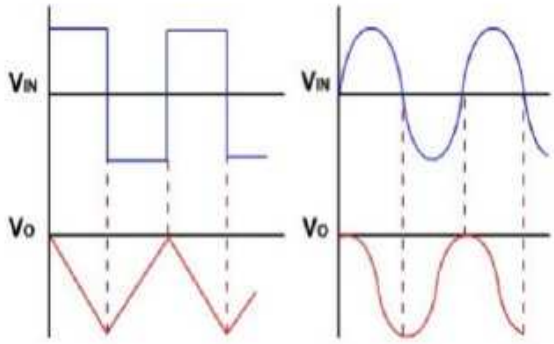
1) Connect the circuit according to the circuit diagram.
2) Apply square wave to the input terminal of integrator circuit.
3) Set the input voltage 1V peak to peak and frequency at 1KHz.
4) Note down the input and output waveform.
5) Draw the waveform on graph paper.

Observation Table:

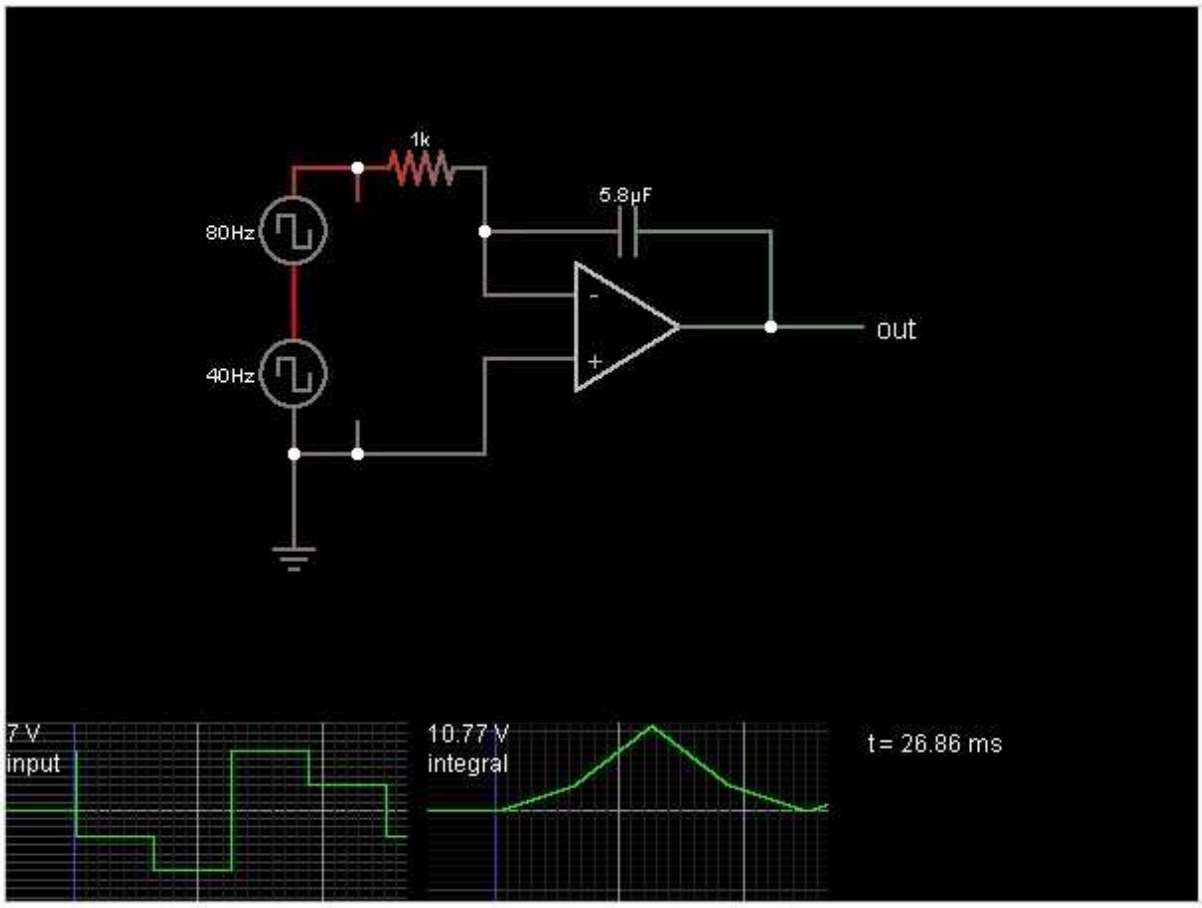
OBSERVATION TABLE: -

S.NO	I/P Voltage Vin	O/P Voltage Vo	Frequency in KHz.	Gain=20log Vo/ Vin

GRAPH:-



Integrator in Simulator Design:



Result: Waveforms shows integrator acts as low pass filter.

Experiment No: 6

AIM: Verify the operation of a voltage comparator circuit using op amp 741.

Apparatus Required: CRO, Function Generator, Bread Board, and 741 IC, ±12V supply, Resistors, and Connecting leads.

Theory:

Voltage Comparator:

A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with output ±Vsat = (Vcc). If the signal is applied to the inverting terminal of the op-amp it is called inverting comparator and if the signal is applied to non-inverting terminal of the op-amp it is called non-inverting comparator. In an inverting comparator if input signal is less than reference voltage, output will be +Vsat. When input signal voltage is greater than reference voltage output will be –Vsat. The vice-versa takes place in non-inverting comparator.

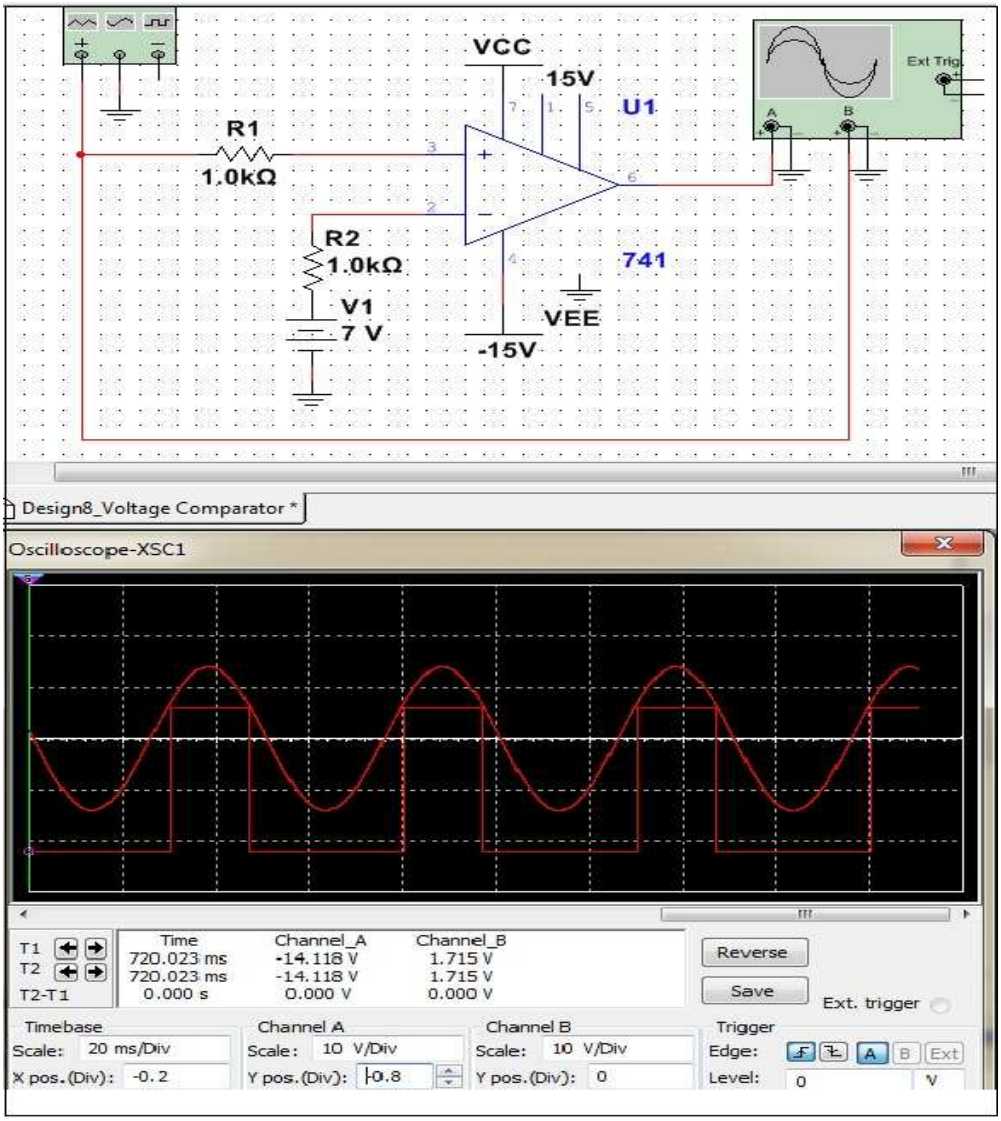
In theory, a standard op-amp operating in open-loop configuration (without negative feedback) may be used as a low-performance comparator. When the non-inverting input (V+) is at a higher voltage than the inverting input (V-), the high gain of the op-amp causes the output to saturate at the highest positive voltage it can output. When the non-inverting input (V+) drops below the inverting input (V-), the output saturates at the most negative voltage it can output. The op-amp's output voltage is limited by the supply voltage. An op-amp operating in a linear mode with negative feedback, using a balanced, split-voltage power supply, (powered by ± V_S) has its transfer function typically written as: $V_{out} = A_o(V_1 - V_2)$. However, this equation may not be applicable to a comparator circuit which is non-linear and operates open-loop (no negative feedback)

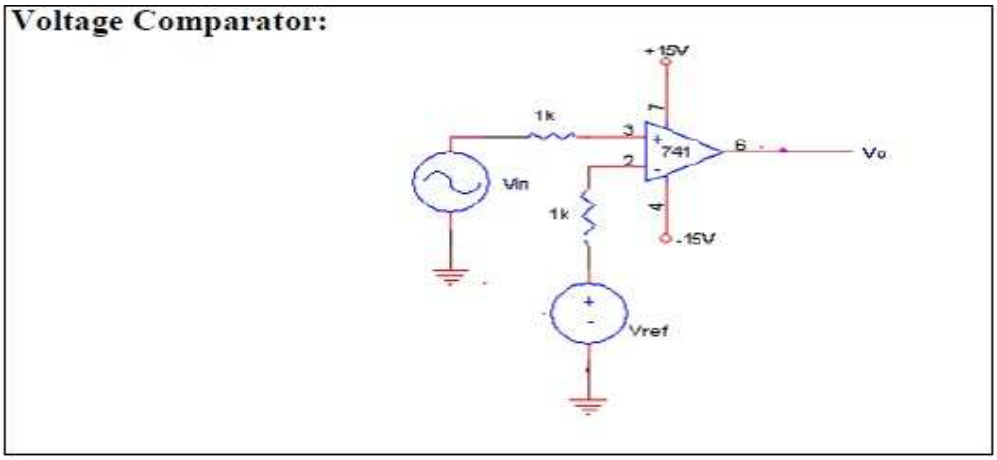
In practice, using an operational amplifier as a comparator presents several disadvantages as compared to using a dedicated comparator.

1. Op-amps are designed to operate in the linear mode with negative feedback. Hence, an op-amp typically has a lengthy recovery time from saturation. Almost all op-amps have an internal compensation capacitor which imposes slew rate limitations for high frequency signals. Consequently an op-amp makes a sloppy comparator with propagation delays that can be as slow as tens of microseconds.
2. Since op-amps do not have any internal hysteresis an external hysteresis network is always necessary for slow moving input signals.
3. The quiescent current specification of an op-amp is valid only when the feedback is active. Some op-amps show an increased quiescent current when the inputs are not equal.
4. A comparator is designed to produce well limited output voltages that easily interface with digital logic. Compatibility with digital logic must be verified while using an op-amp as a comparator.
5. Some multiple-section op amps may exhibit extreme channel-channel interaction when used as comparators.

6. Many opamps have back to back diodes between their inputs. Opamp inputs usually follow each other so this is fine. But comparator inputs are not usually the same. The diodes can cause unexpected current through inputs.

Circuit Diagram:



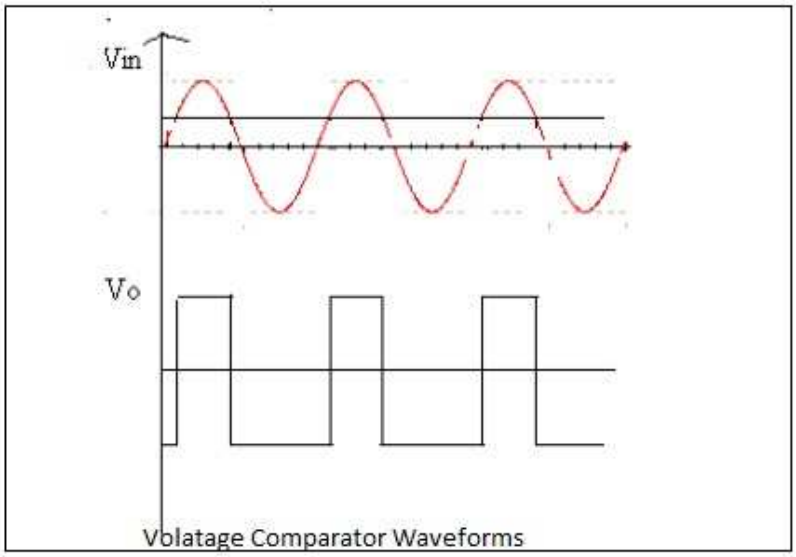


Procedure:

Voltage comparator:

1) Connect the circuit as shown in the figure
2) Connect an alternating waveform to the non-inverting input of the op-amp
3) Connect a reference voltage source to inverting input of the op-amp
4) Plot the input and output waveform.

Wave form:



RESULT:
Thus, the use of op-amp as voltage comparator was studied.

Experiment No: 7

AIM: Verify the operation of a zero crossing detector circuit using op amp 741.

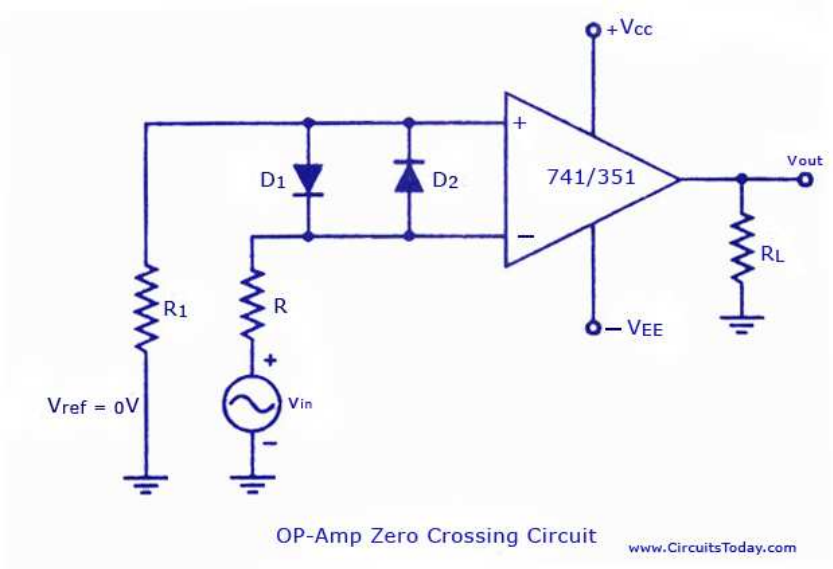
Apparatus Required: CRO, Function Generator, Bread Board, and 741 IC, ±12V supply, Resistors and Connecting leads.

Theory:

Zero Crossing Detectors:

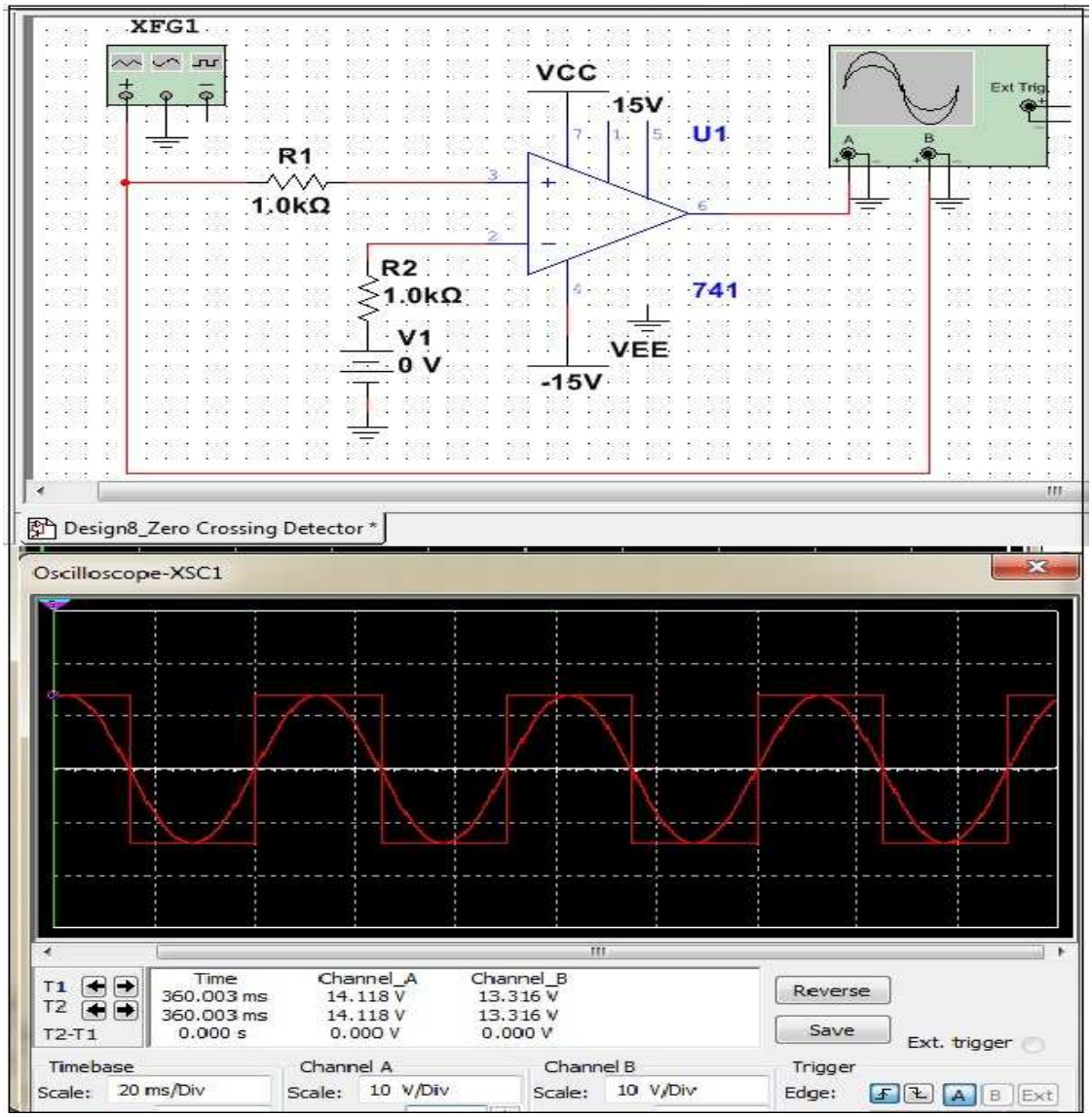
Zero crossing comparator (ZCD) is an application of voltage comparator. It converts any time varying signal to square of same time period with amplitude ±Vsat. The reference voltage is set as zero volts. When the polarity of the input signal changes, output square wave changes polarity.

Zero-crossing detector is an applied form of comparator. Either of the op-amp basic comparator circuits discussed can be employed as the zero-crossing detector provided the reference voltage V_{ref} is made zero. Zero-crossing detector using inverting op-amp comparator is depicted in figure. The output voltage waveform shown in figure indicates when and in what direction an input signal v_{in} crosses zero volt.

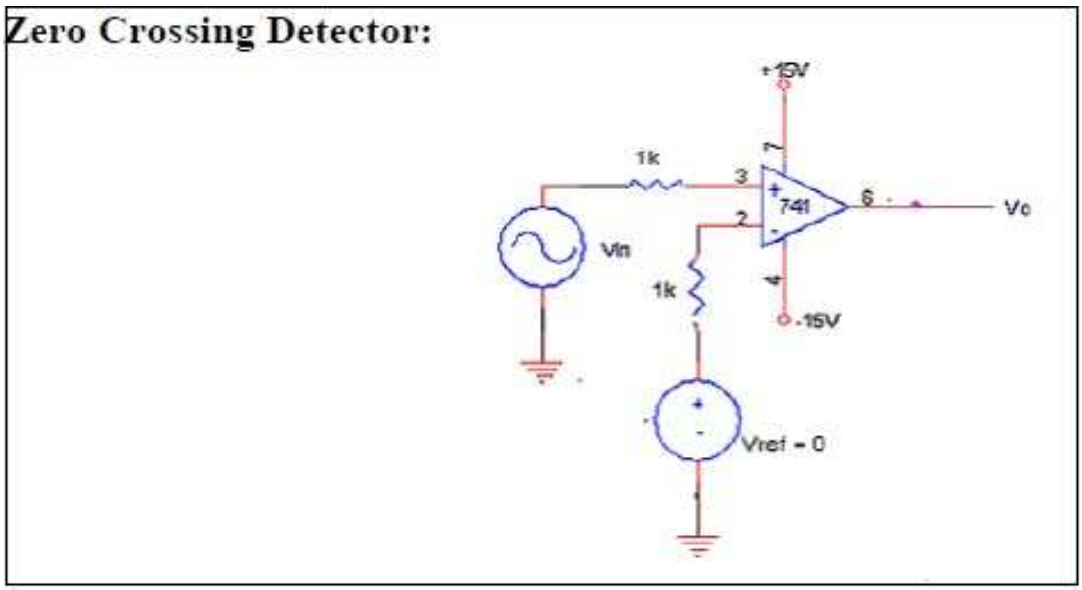


In some applications the input signal may be low frequency one (i.e. input may be a slowly changing waveform). In such a case output voltage v_{OUT} may not switch quickly from one saturation state to the other. Because of the noise at the input terminals of the op-amp, there may be fluctuation in output voltage between two saturation states (+ V_{sat} and – V_{sat} voltages). Thus zero crossings may be detected for noise voltages as well as input signal v_{in}. Both of these problems can be overcome, if we use regenerative or positive feeding causing the output voltage v_{out} to change faster and eliminating the false output transitions that may be caused due to noise at the input of the op-amp.

Circuit Diagram:



Zero Crossing Detector:

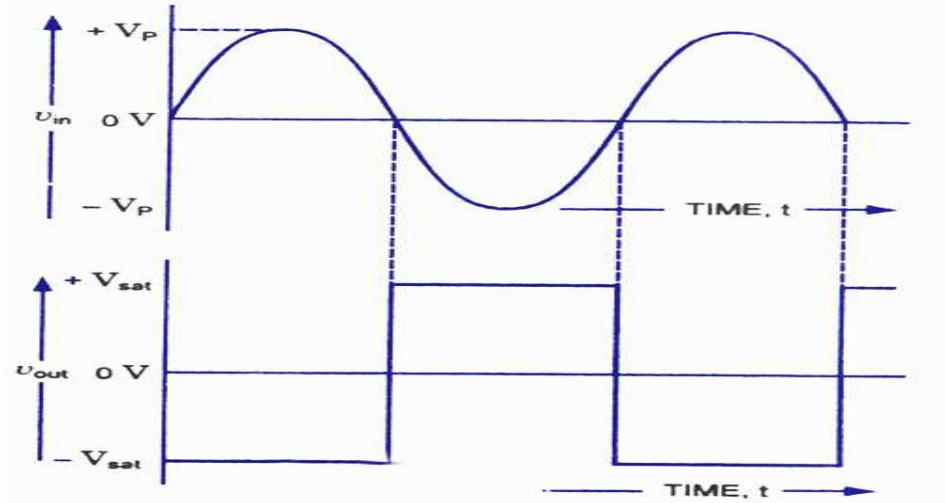


Procedure:

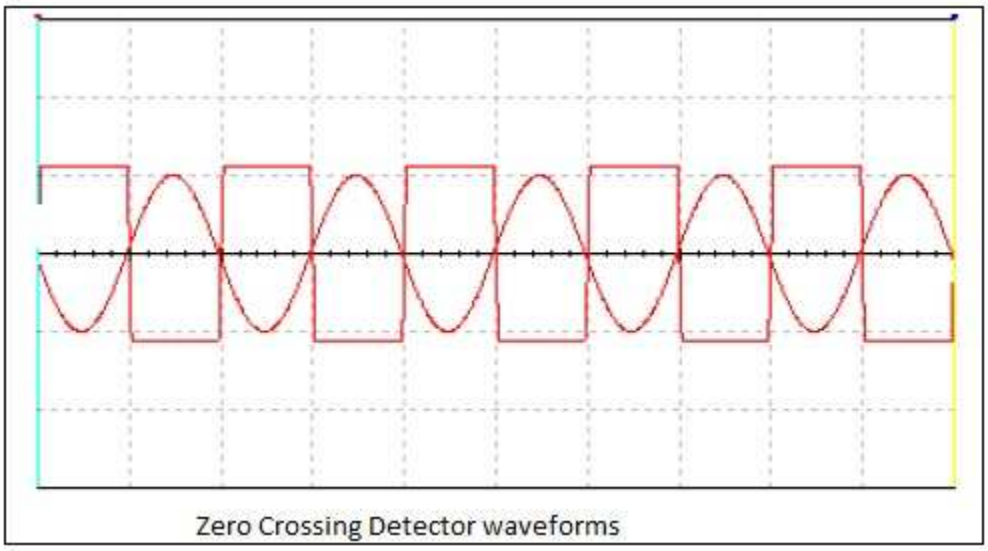
Zero crossing detectors:

1) Connect the circuit as shown in figure
2) Connect the input to a signal generator generating a sin wave with one volt peak to peak at 1 kHz.
3) Connect the input and output to dual channel CRO and compare the input and output.
4) Plot the input and output waveform in a graph.

Wave form:



Input and Output Waveforms



Zero Crossing Detector waveforms

RESULT:

Thus, the use of op-amp as zero crossing detectors was studied.

Experiment No: 8

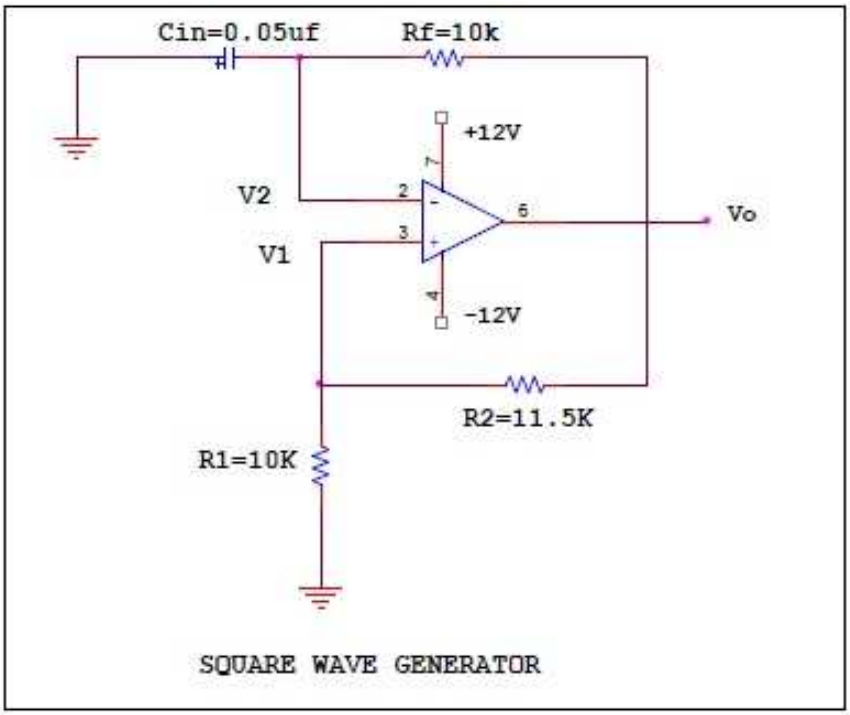
AIM: To design and realize using op amp 741, square wave generator.

Apparatus Required: CRO, Function Generator, Power supply, Bread Board, 741 IC, Resistors, capacitor and connecting leads.

Theory:

Square waves are generated when the op-amp is forced to operate in the saturation region. That is, the output of the op amp is forced to swing respectively between +Vsat and –Vsat. Resulting in the generation of square wave. The square wave generator is also called a free –running or astable multivibrator. Assuming the voltage across capacitor C is zero at the D.C. supply voltage +Vcc and –VEE are applied. Initially the capacitance C acts, as a short circuit. The gain of the op-amp is very large hence V1 drives the output of the op-amp to its saturation

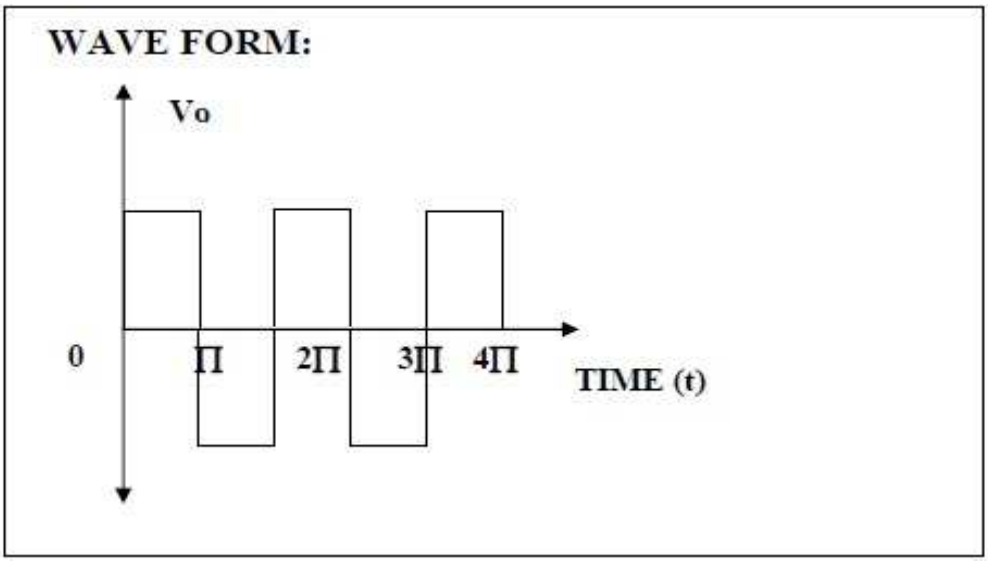
Circuit Diagram:



Procedure:

1) Connect the circuit as shown in figure.
2) Switch on the power supply.
3) No. Input signal is feed from function generator. It is self generating.
4) Frequency can be varied by changing RC combination.
5) Output is obtained at pin 6 of op-amp.

Wave forms:



Result: Squire Wave is obtained on CRO.

Experiment No: 9

AIM: Study of IC 555 as astable and monostable multivibrator.

Apparatus Required: IC 555, CRO, Function Generator, Bread Board, Resistors, capacitor and connecting leads.

Theory:

555 Timer - An 8 pin IC designed for use in a variety of switching applications.
Multivibrator - A circuit designed to have zero, one, or two stable output states. There are three types of multivibrators:

1) Astable (or Free-Running Multivibrators)
2) Monostable (or One-Shot)
3) Bistable (or Flip- Flop)

1). Astable multivibrator – A switching circuit that has no stable output state. The astable multivibrator is a rectangular wave oscillator. Also referred to as a free-running multivibrator.

The IC555 timer is a 8 pin IC that can be connected to external components for astable operation. The simplified block diagram is drawn. The OP-AMP has threshold and control inputs. Whenever the threshold voltage exceeds the control voltage, the high output from the OP –AMP will set the flip-flop. The collector of discharge transistor goes to pin 7. When this pin is connected to an external trimming capacitor, a high Q output from the flip flop will saturate the transistor and discharge the capacitor.

When Q is low the transistor opens and the capacitor charges. The complementary signal out of the flip-flop goes to pin 3 and output. When external reset pin is grounded it inhibits the device. The on – off feature is useful in many application. The lower OP- AMP inverting terminal input is called the trigger because of the voltage divider. The non-inverting input has a voltage of +Vcc/3, the OP-Amp output goes high and resets the flip flop.

The output frequency is,

$f = 1.44/(RA + RB)C$

The duty cycle is,

$D = RB / (RA + 2RB) * 100\%$

The duty cycle is between 50 to 100% depending on RA and RB.

2).Monostable multivibrator – A switching circuit with one stable output state. Also referred to as a one-shot. The one-shot produces a signal output pulse when it receives a valid input trigger signal.

This circuit is a monostable multivibrator, or one-shot, made with a 555 timer chip. Click the logic input on the left (the "H"), and the output goes high for a short time, and then it goes

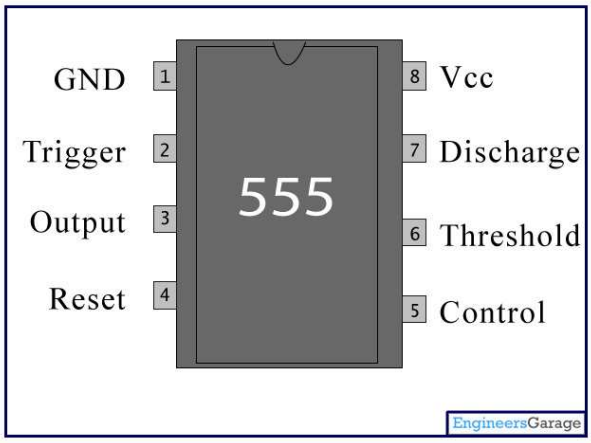
low_again.

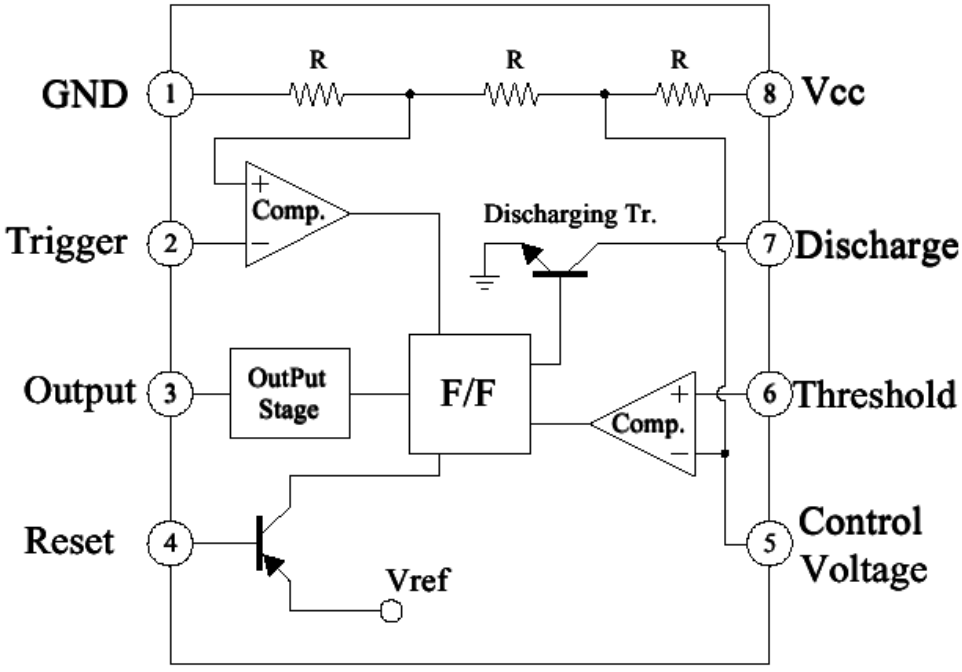
A timing interval starts when the trigger input ("tr") is brought low. When this happens, the 555 output goes high. This causes the capacitor to be charged until it reaches 6.67V. Then, the timing interval ends, the output goes low, and the capacitor is discharged through the "dis"input.

The capacitor in front of the trigger input causes the monostable to be negative-edge triggered. If the capacitor is replaced with a wire, and the logic input is held low too long, then the 555's output will start to oscillate.

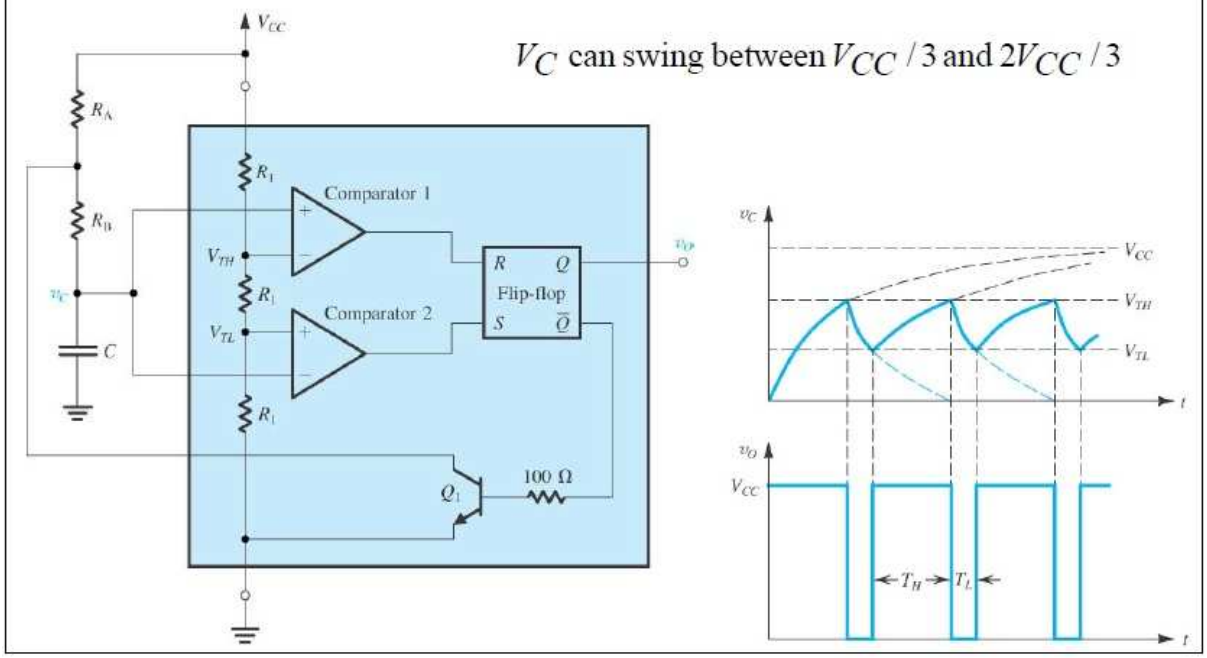
3).Bistable multivibrator – A switching circuit with two stable output states. Also referred to as a flip-flop. The output changes state when it receives a valid input trigger signal, and remains in that state until another valid trigger signal is received.

Diagram:





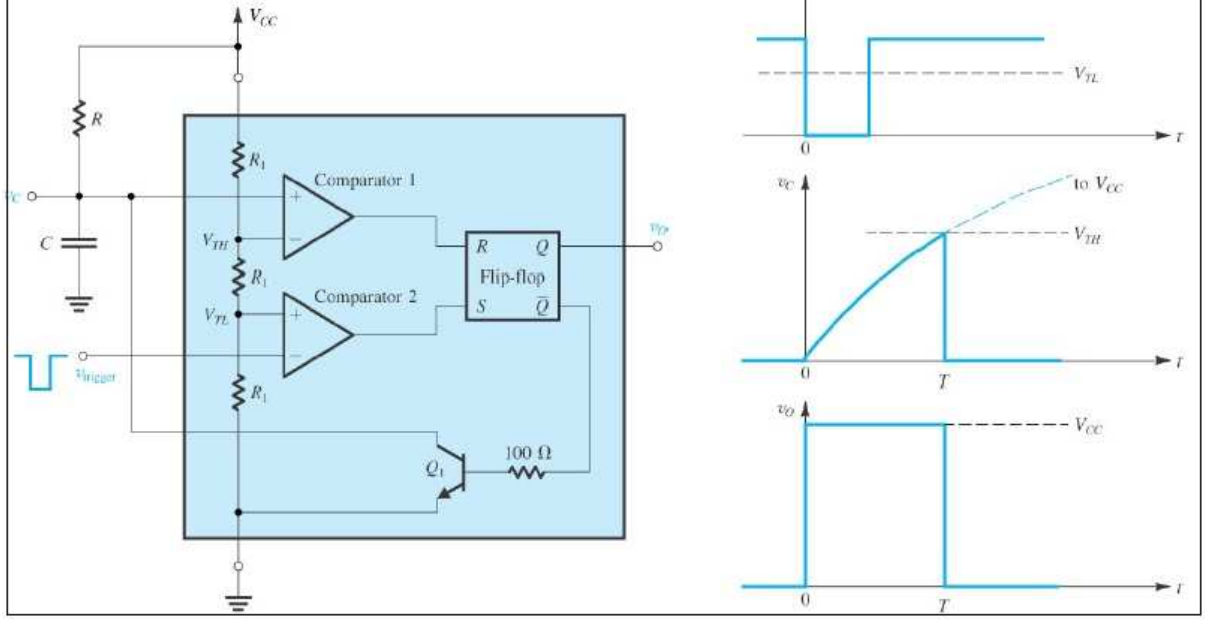
An Astable Multivibrator Using the 555 IC



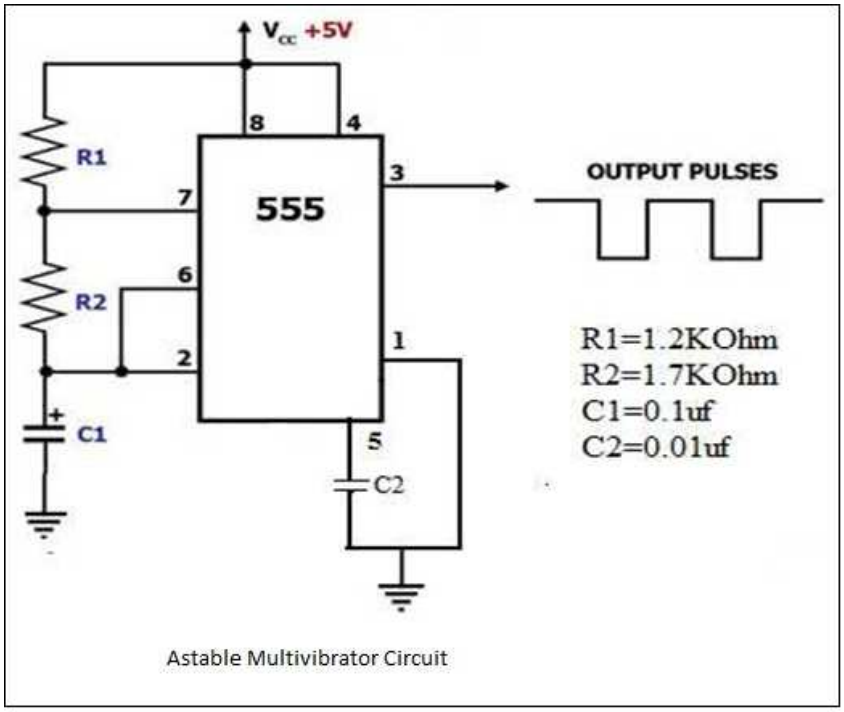
Implementing a Monostable Multivibrator Using the 555 IC

$$v_c = V_{CC}(1-e^{-t/RC}); v_c = V_{TH} = \frac{2}{3}Vcc \text{ at } t = T$$

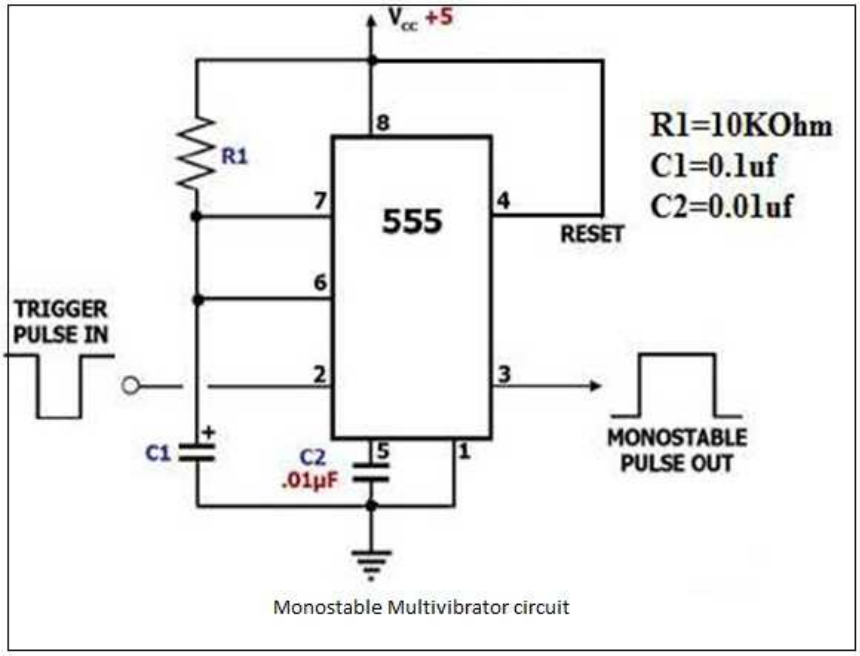
$$T = CR\ln 3 = 1.1CR$$



Practical Circuit Diagram:



Astable Multivibrator Circuit



Monostable Multivibrator circuit

Procedure:

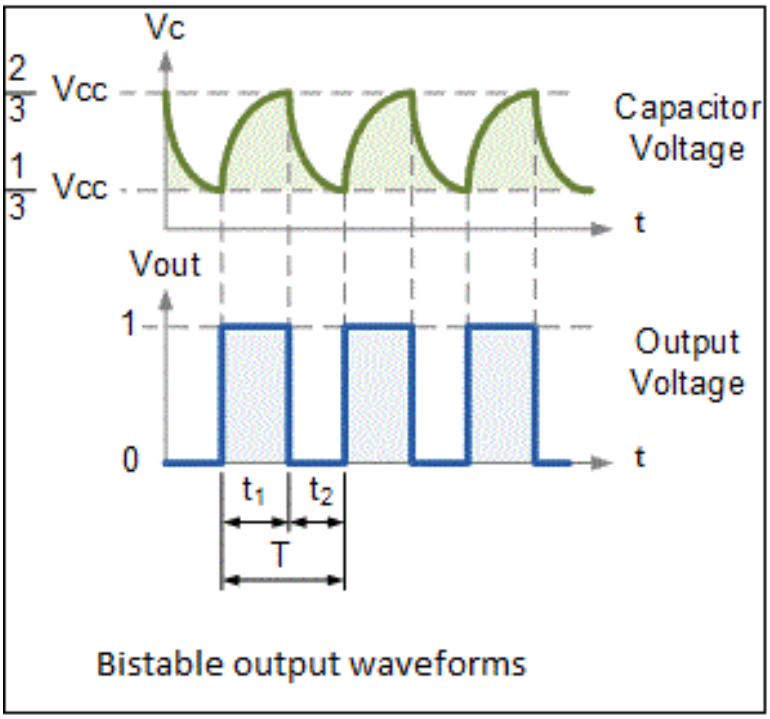
Astable multivibrator:

1) Connect the circuit using the component values as per the design.
2) Observe and sketch the capacitor voltage wave form (pin-6) and output waveform (pin-3) measure the frequency and duty cycle of the output wave form
3) Connect the circuit of fig using component values as per the design and repeat the step 2 by adjusting both the potential meters for duty cycle of 10%, 50% and 90% with a frequency of 1 kHz.

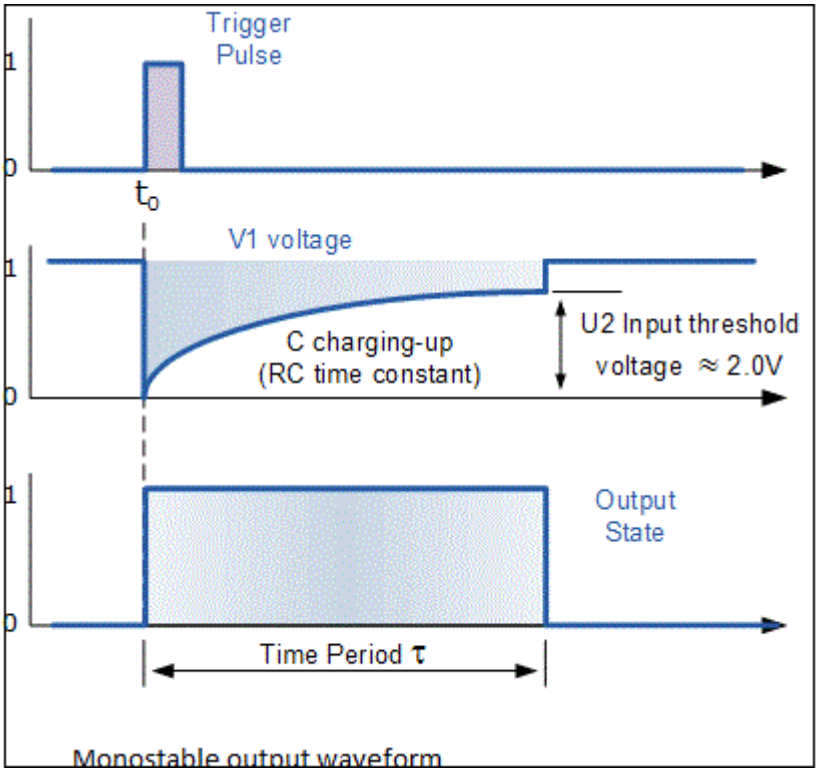
Monostable Multivibrator:

1) Connect the circuit using the component values as per the design
2) Set the square wave 2.5V peak and 1KHz trigger input on function generator
3) Apply the trigger input at pin-2 through capacitor C1. Observe both trigger input and the output of the multivibrator on CRO simultaneously and sketch the waveforms
4) Repeat the step 3 for trigger input of 2KHz frequency

Wave forms:



Bistable output waveforms



Result: Astable and monostable multivibrator has been studied.

Experiment No: 10

AIM: To study the operation of IC723 voltage regulator

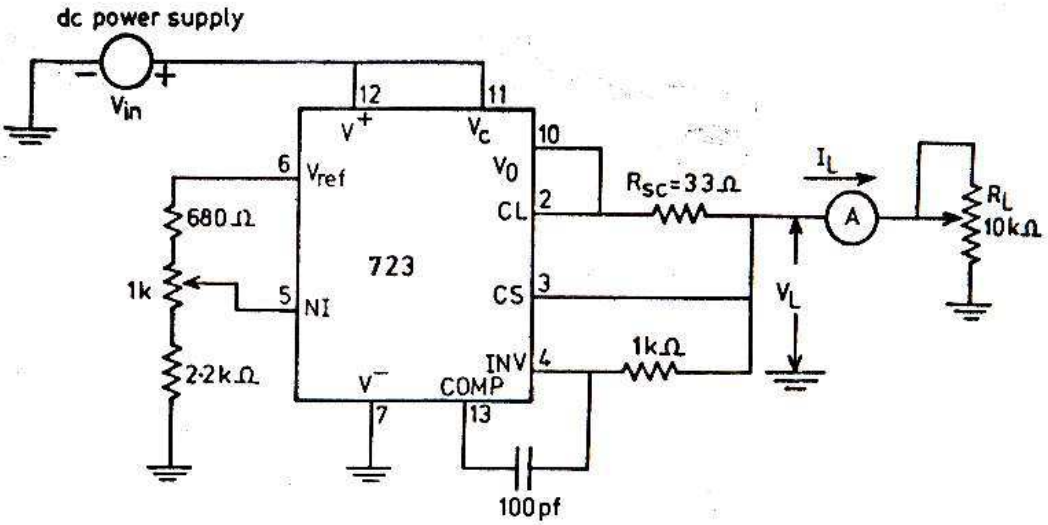
Apparatus Required: DC power supply, Digital Multimeter, Ammeter, Bread Board Components

1. 1kΩ Resistor – 1 No.
2. 33Ω Resistor – 1 No.
3. 10k Ω Resistor – 1 No
4. 680 □ Resistor – 1 No.
5. 2.2 k□ Resistor – 1 No.
6. 100 pF Capacitor – 1 No
7. IC723

Theory:

The three-terminal regulators have the following limitations
1. No short-circuit protection
2. Output voltage (+ve or –ve) is fixed

These limitations have been overcome in 723 general purpose regulator. This IC is inherently low current device but can be boosted to provide 5 amps or more current by connecting external components. The limitation of 723 is that it has no in-built thermal protection. It also has no short-circuit current limits. The IC723 has two sections. The first section consists of Zener Diode constant current source and a reference amplifier. The other section of the IC consists of an error amplifier series pass transistor and a current limit transistor. This is a 14-pin DIP package. The main Features of 723 include an input voltage of 40v max, output voltage is adjustable from 2V to 37V, 150 mA output current without external pass resistor, can be used as either a linear or a switching regulator.



723 voltage regulator

Procedure:

1. Connect the 723 regulator as shown in the circuit diagram
2. Set Dc power supply voltage Vin to +10V measure and record Vref with respect to ground. With load RL(10k□ pot) removed from the circuit (output open). Measure the minimum and maximum output voltage by rotating the 1k□ pot through its full range.
3. Now adjust the 1k□ pot so that Vo is +5V dc. Measure the voltage between the wiper arm of the 1 k□ pot and ground.
4. Adjust the load RL (10 k□) pot until the load current IL = 1 mA. Record VL. Repeat for different values of load currents 5mA, 10mA, 15mA, 18mA. Calculate the load regulation and compare with manufacturer's specifications
5. Gradually increase the load current above 18mA, you will see that the load voltage suddenly decreases when the load current is about 18 to 20 mA. Now the voltage across RSC is enough to begin current limiting. Measure and record a few values of load current and load voltage below and above the current limiting point. Plot a graph of VL vs IL from the data obtained in steps 4 and 5

Observations:

1. The load regulation = _____ %
2. The line regulation = _____%

Calculations:

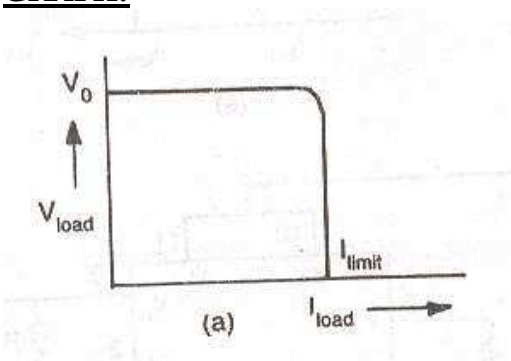
1. The load regulation can be calculated by using the below formulae

$$\%\text{load regulation} = ((V_{fl} - V_{nl}) / (V_{fl})) * 100$$

2. The line regulation can be calculated by using the below formulae

$$\%\text{line regulation} = (\Delta V_o / \Delta V_i)$$

GRAPH:



RESULT:

i.The % load regulation =
ii. The % line regulation =

INFERENCE:

i. The working of 723 regulator is observed and the output is plotted.
ii. The load regulation is calculated
iii. The line regulation is calculated

Experiment No: 11

AIM: To study the operation of NE565 PLL and use NE565 as a multiplier.

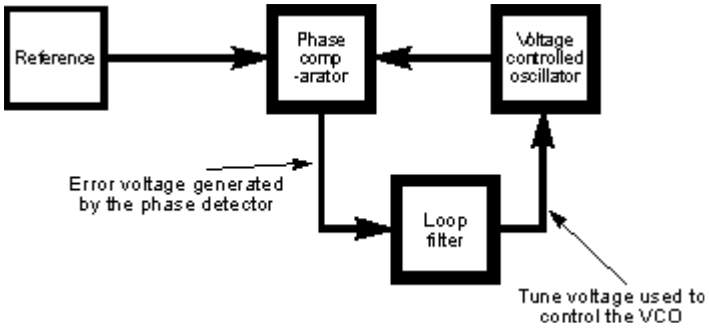
Apparatus: DC power supply, CRO, Bread Board, Function Generator, Resisters, Capacitors, and IC 565

Theory:

Phase locked loop operation

The basic concept of the operation of the PLL is relatively simple, although the mathematical analysis and many elements of its operation can become more complicated

The Voltage Controlled Oscillator, VCO, within the PLL produces a signal which enters the phase detector. Here the phase of the signals from the VCO and the incoming reference signal are compared and a resulting difference or error voltage is produced. This corresponds to the phase difference between the two signals.



Block diagram of a basic phase locked loop (PLL)

The error signal from the phase detector passes through a low pass filter which governs many of the properties of the loop and removes any high frequency elements on the signal. Once through the filter the error signal is applied to the control terminal of the VCO as its tuning voltage. The sense of any change in this voltage is such that it tries to reduce the phase difference and hence the frequency between the two signals. Initially the loop will be out of lock, and the error voltage will pull the frequency of the VCO towards that of the reference, until it cannot reduce the error any further and the loop is locked.

When the PLL, phase locked loop, is in lock a steady state error voltage is produced. By using an amplifier between the phase detector and the VCO, the actual error between the signals can be reduced to very small levels. However some voltage must always be present at the control terminal of the VCO as this is what puts onto the correct frequency.

The fact that a steady error voltage is present means that the phase difference between the reference signal and the VCO is not changing. As the phase between these two signals is not changing means that the two signals are on exactly the same frequency.

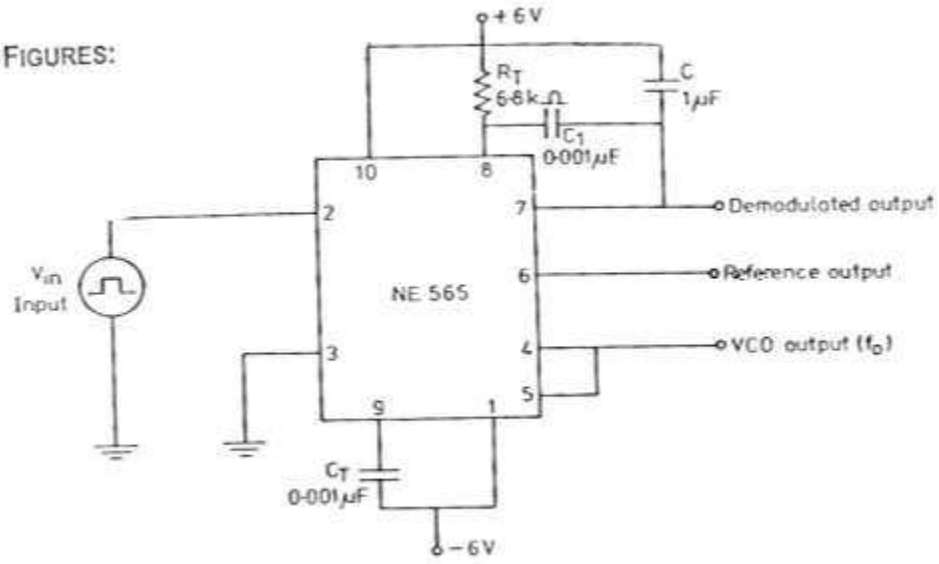
The 565 is available as a 14-pin DIP package. It is produced by Signatic Corporation. The output
Frequency of the VCO can be rewritten as:

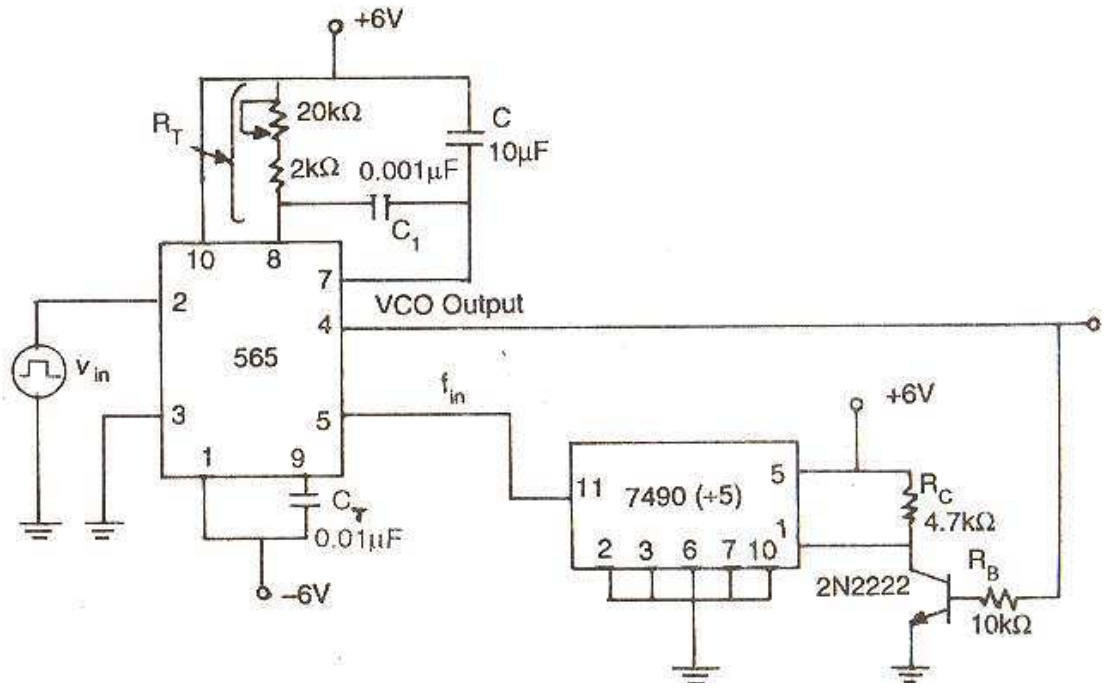
Fo= (0.25/Rt Ct) Hz

Where RT and CT are the external resistor and capacitor connected to pin 8 and pin 9. A value between 2 kΩ and 20 kΩ is recommended for RT. The VCO free running frequency is adjusted with RT and CT to be at the centre fo the input frequency range.

Circuit Diagram:

FIGURES:





Procedure:

1) Connect the circuit using the component values as shown in the figure
2) Measure the free running frequency of VCO at pin 4 with the input signal Vin set = zero. Compare it with the calculated value = 0.25/ RTCT
3) Now apply the input signal of 1Vpp square wave at a 1kHz to pin 2
4) Connect 1 channel of the scope to pin 2 and display this signal on the scope
5) Gradually increase the input frequency till the PLL is locked to the input frequency. This frequency f1gives the lower ends of the capture range. Go on increase the input frequency, till PLL tracks the input signal, say to a frequency f2. This frequency f2 gives the upper end of the lock range. If the input frequency is increased further the loop will get unlocked.
6) Now gradually decrease the input frequency till the PLL is again locked. This is the frequency f3, the upper end of the capture range. Keep on decreasing the input frequency until the loop is unlocked. This frequency f4 gives the lower end of the lock range
7) The lock range $\Delta fL = (f2 - f4)$ compare it with the calculated value of $(\pm 7.8fo/12)$
   Also the capture range is $\Delta fc = (f3 - f1)$. Compare it with the calculated value of capture range.
   $\Delta fc = \pm (\Delta fL/(2\square)(3.6)(10^3)Xc)^{1/2}$
8) To use PLL as a multiplie5r, make connections as show in fig. The circuit uses a 4-bit binary counter 7490 used as a divide-by-5 circuit.
9) Set the input signal at 1Vpp square wave at 500Hz
10) Vary the VCO frequency by adjusting the 20KΩ potentiometer till the PLL is locked. Measure the output frequency
11) Repeat step 9 and 10 for input frequency of 1 kHz and 1.5 kHz.

Observations:

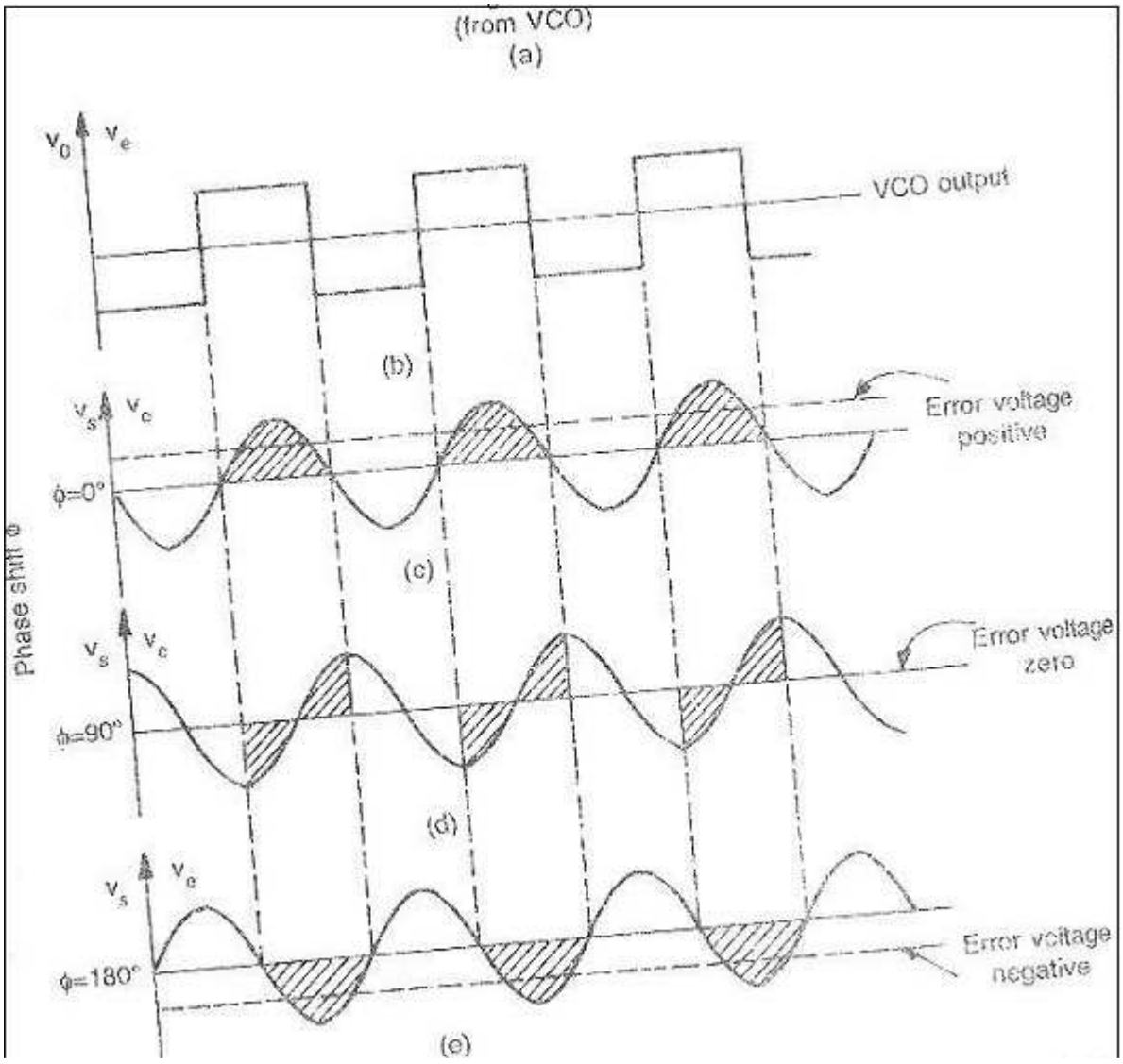
fo = _____
fL = _____
fC = _____

Calculations:

$\Delta fL = (f2 - f4) = (\pm 7.8fo/12)$

$\Delta fc = \pm (\Delta fL/(2\square)(3.6)(10^3)Xc)^{1/2}$

Graph:



Result:

fo = _____

fL = _____

fC = _____

Inference:

- The working of 565 PLL is observed and the output is plotted.
- The time period of the output waveform is calculated.
- Frequency of the output wave form is calculated.
- The Lock range and Capture range of the PLL are calculated.