

Audio Engineering Society

Convention Paper

Presented at the 124th Convention 2008 May 17–20 Amsterdam, The Netherlands

The papers at this Convention have been selected on the basis of a submitted abstract and extended precis that have been peer reviewed by at least two qualified anonymous reviewers. This convention paper has been reproduced from the author's advance manuscript, without editing, corrections, or consideration by the Review Board. The AES takes no responsibility for the contents. Additional papers may be obtained by sending request and remittance to Audio Engineering Society, 60 East 42nd Street, New York, New York 10165-2520, USA; also see www.aes.org. All rights reserved. Reproduction of this paper, or any portion thereof, is not permitted without direct permission from the Journal of the Audio Engineering Society.

A Digitally Direct Driven Dynamic-type Loudspeaker

Ryota Saito¹, Akira Yasuda², Kazusige Kuroki³, Tomohiro Tsuchiya⁴, and Naoto Shinkawa⁵

- ¹ Hosei University, Koganei, Tokyo, 182-0002, Japan ryota.saito.66@gs-eng.hosei.ac.jp
- ² Hosei University, Koganei, Tokyo, 182-0002, Japan yasuda@hosei.ac.jp
- ³ Hosei University, Koganei, Tokyo, 182-0002, Japan i06r3109@k.hosei.ac.jp
- ⁴ Hosei University, Koganei, Tokyo, 182-0002, Japan c04d3066@k.hosei.ac.jp
- ⁵ Hosei University, Koganei, Tokyo, 182-0002, Japan c04d3050@k.hosei.ac.jp

ABSTRACT

If a speaker can be driven digitally, all processes from the input to the output can be performed digitally without the use of analog components such as power amplifiers, and a small, light, and high-quality speaker system can be realized. In this paper, we propose the basic principle behind Digital-Speaker, and a digitally driven dynamic-type loudspeaker provided with multiple voice coils employing multibit delta-sigma modulation. The piezoelectric-speaker used in our previous study is replaced by the voice coil. The prototype is implemented along with a FPGA, CMOS drivers, and a dynamic-type loudspeaker. The THD and SPL are approximately 0.1% and 104 dB, respectively, and the output power is 1 W even when the power supply voltage is 1 V.

1. INTRODUCTION

Most of the audio systems are realized by using a digital system because the audio signals are stored in the

form of digital data on storage media such as CDs and DVDs. However, a loudspeaker is an analog device.

The digital audio signals are converted into analog signals by using a digital-to-analog converter (DAC).

The loudspeaker is driven by a heavy analog amplifier connected to the DAC. As compared to the components of a digital circuit, these analog devices are usually large in size at the circuit scale and also heavy. Hence, class-D amplifiers are becoming popular due to their light weight and their ability to reduce the power dissipation. However, the conventional digital class-D amplifiers require a clock signal of frequency exceeding 100 MHz. The quantization noise in a 1-bit delta-sigma modulator (DSM) employed to realize a switching amplifier results in large out-of-band noise.

Furthermore, a distortional characteristic is not suitable for the advanced audio systems. If the speaker system can be directly driven by a digital signal, the DAC and heavy analog amplifier can be eliminated from the audio system.

We have proposed a speaker system (Digital-SP) directly driven by a digital signal in the 121st AES convention [1]. In the proposed system the bit length of the input digital data is reduced by a multibit DSM in order to realize Digital-SP by using a few loudspeaker subunits. The output binary code is converted into a thermometer code in order to drive equal-weighted subloudspeakers by using an ON-OFF control circuit.

The advantages of using Digital-SP along with our method are given below.

- -All the electrical systems employ digital processing (analog circuits are not necessary).
- -The loudspeaker subunits are driven by ON-OFF signals.
- -The power efficiency is high.
- -The effect of nonlinearity in the driven circuit is small.
- -The out-of-band noise is reduced by the multibit DSM.

In this study, we propose a novel digital speaker system that can directly drive the speaker units. A prototype digital speaker implemented along with a FPGA, CMOS drivers, and loudspeaker subunits will be discussed.

2. CONVENTIONAL SPEAKER SYSTEM

The block diagram of a conventional audio system including a speaker is shown in Fig.1. The output PCM signal from a CD player (or a digital audio player) is converted into an analog signal by the DAC. Because the level of the converted signal is relatively low, it must be amplified. The analog signal from the DAC is amplified by an analog amplifier. Through the analog speaker cable, the output signal is outputted from the speaker as sound. Considering that the digital signal is finally converted into an analog signal, the speaker can be recognized as a part of the DAC. The performance requirements of the speaker are listed below.

- The level of distortion should be low.
- The signal/noise ratio (SNR) should be high.
- The dynamic range should be high.
- The frequency characteristics should be flat and spread over a wide range.

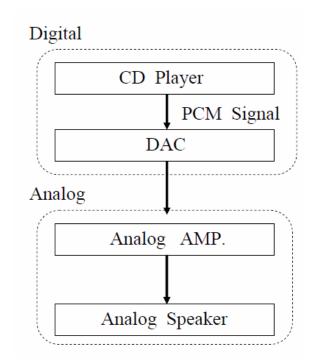


Figure 1: Conventional audio system.

Analog devices such as analog amplifiers are usually large in size and heavy. Therefore, if the speaker can be driven digitally, all the processes from the input to the output can be performed digitally.

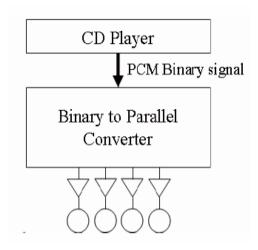


Figure 2: Architecture of digital speaker system.

3. DIGITAL SPEAKER SYSTEM

The architecture of the proposed system is shown in Fig.2. In this system, the analog power amplifier and other analog components are not used, and a small, light, and high-quality speaker can be realized.

The conventional digitally driven speaker utilizes binary weighted subunits in order to realize digital to analog conversion. Since the coefficient of the weighted value directly determines the overall performance of the speaker system, the quality is limited by the electrical and/or mechanical accuracy. In the proposed system, equal-weighted loudspeaker subunits are only used. Therefore, the electrical and mechanical accuracy can be improved.

However, if the equal-weight loudspeaker subunits are used, the SNR of the digital speaker is limited by the number of the loudspeaker subunits. A method to improve the SNR is required for this system. The conventional class-D amplifier employs the PWM modulation to reduce the resolution of amplitude to 1 bit. A high-frequency clock signal, however, is required to increase the time-domain resolution.

The block diagram of the proposed digital speaker system is shown in Fig.3. The digital data from the CD player, 16-bit LR digital data streams, are converted into multibit signals by the multibit DSM. The quantization noise caused by the reduction in the bit length is shifted towards a higher frequency. Therefore, a higher SNR, exceeding 98 dB, can be realized. The output data from the DSM is converted to equal-weighted signals, which drive the speakers with the CMOS buffers, by a binaryto-thermometer code converter. The performance of the speakers should be the same in order to reproduce the original signal. However, actual devices exhibit a performance mismatch that is caused by the manufacturing error. The mismatch degrades the sound quality drastically. For example, a sound pressure mismatch of 1% reduces the SNR to 40 dB.

In order to reduce the degradation, a mismatch shaper circuit is placed between the binary-to-thermometer-code converter and the CMOS buffer (Fig.4). The mismatch shaper shifts the noise to a higher frequency, beyond the audio frequency range. If the mismatch of the speaker is large, a high-order mismatch shaper circuit is required.

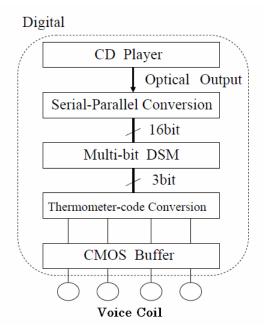


Figure 3: Block diagram of digital speaker.

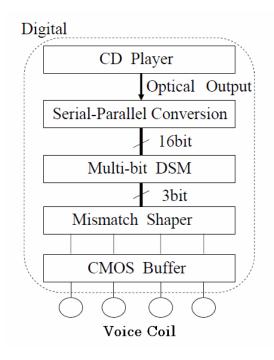


Figure 4: Block diagram of digital speaker with mismatch shaper.

3.1. Delta-sigma Modulation

In this study, we use a multibit (third-order) DSM (Fig.5) that has a steep noise-shaping characteristic.

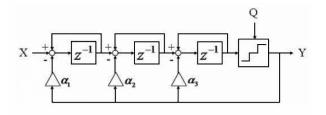


Figure 5: Block diagram of third-order DSM.

Adjusting the parameters α_1 , α_2 , and α_3 in the diagram equal to 1, 3, and 3, respectively, the following equation (1) is obtained.

$$Y = X + (1 - Z^{-1})^3 Q \tag{1}$$

where Q is the quantization noise of an internal quantizer. This equation indicates the third-order noise shaping. If the number of levels is increased, the quantization noise can be reduced. Thus, the performance of the digital speaker improves with the increase in the number of loudspeaker subunits. In addition, the sound pressure also increases. Thus, low voltage and high power can be realized by using the proposed method.

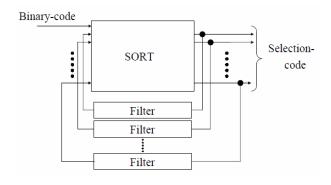


Figure 6: Block diagram of high-order mismatch shaper circuit.

3.2. Proposed Method

In this study, we propose a loudspeaker with multiple voice coils and a Digital-SP system using multiple-voice-coil loudspeakers.

The conventional dynamic loudspeaker converts analog electric signals into mechanical displacements by using the voice coils under a magnetic field.

On the contrary, the multiple voice coils in the prototype digital dynamic speaker are directly driven by the digital signals. This is completely different from the mode of operation of the conventional loudspeaker. The voice coils are driven by the mismatch shaper circuit in order to reduce the mismatch effects caused by position of the voice coils. The mechanical displacement of a diaphragm (voice coil) is controlled depending on the net magnetic flux generated by the voice coils. High performance can be realized because the mismatch in the magnetic flux generated by the voice coils is small and the noise caused by the mismatch is reduced by the mismatch shaper circuit. In addition, there is no

degradation caused by the placement of the loudspeaker subunits such piezoelectric-type loudspeakers.

As compared to the output power obtained with the piezoelectric-type loudspeaker, the output power of the proposed speaker can be easily increased. Since multiple voice coils are used, the output power is multiplied by a factor equal to the number of coils. The output power of this speaker is considerably higher than that of the conventional loudspeaker. Therefore, a high-power speaker system can be realized without a DC-DC converter, even if the power supply voltage is low. An output power of 1 W can be realized with a 1-V power supply by using the proposed Digital-SP (the impedance of the voice coil is 4 Ω), although the output power of the conventional speaker system is 0.125 W.

3.3. Mismatch Shaper Circuit

In order to improve the accuracy of the internal DAC, some first-order mismatch-shaping techniques have been proposed for the noise caused by the DAC element mismatch [2]–[4].

If the mismatch of the speakers is large, the noise caused by the mismatch cannot be sufficiently reduced. This is because the first-order mismatch shaper circuit can reduce the noise only by 9 dB when the oversampling ratio is doubled. Therefore, a high-order mismatch shaper circuit is required.

Several high-order mismatch shaping techniques, which are extensions of the first-order noise-shaping techniques, have also been proposed and analyzed [4]. The block diagram of the high-order mismatch shaper circuit is shown in Fig.6. The selection codes, which drive the speakers, are determined by the ascending order of the value of the filtered selection code in order to maintain the same values. If the filter is a cascaded integrator, high-order mismatch shaping can be realized. This is an advanced technique and can be used to shape the noise to a higher order; however, it requires significantly a large number of components to implement a vector quantizer when the number of loudspeaker subunits is increased. Nowadays, an advanced CMOS technology allows to utilize the higher order mismatch shaper.

3.4. CMOS Buffer

The output power of the speaker is increased by a push-pull buffer. The driver circuit can be simply realized by using CMOS inverters, as shown in Fig.7.

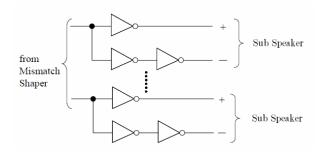


Figure 7: Circuit diagram of CMOS buffer.

3.5. Dynamic Speaker

Eight voice coils are used as loudspeaker subunits of the Digital-SP system. The structure of the proposed digital speaker unit is shown in Fig.8. The eight voice coils are placed on a core. The top view and side view of the prototype speaker unit are shown in Fig.9 and Fig.10, respectively.

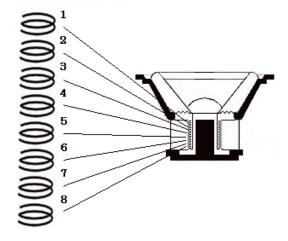


Figure 8: Structure of dynamic speaker.



Figure 9: Photograph of dynamic speaker unit (top view).



Figure 10: Photograph of dynamic speaker unit (side view).

3.6. Piezoelectric Speaker

In the 121st AES convention, we had proposed Digital-SP, a piezoelectric speaker, which was used as the loudspeaker subunits [1]. The loudspeaker subunits were arranged on a plane surface so that output signals of the loudspeaker subunits could be added up, as shown in Fig.11.

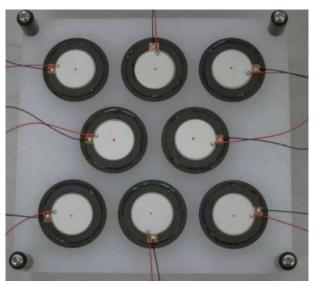


Figure 11: Photograph of piezoelectric speaker unit.

4. EXPERIMENT RESULT

The prototype digital speaker system using the proposed method is implemented along with a FPGA board, CMOS inverters, and a dynamic speaker with multiple voice coils, which are connected with the CD player through SPDIF. The block diagram of the prototype digital speaker system is shown in Fig.12. The digital audio data from the CD player is converted into 16-bit LR channel PCM data, which is inputted to an interpolation digital filter in order to upsample the data and attenuate an image signal. The upsampled signal is inputted to a 4-bit (9-level) DSM, so that the output bit length is reduced to 4 bits in order to drive the loudspeaker subunits. The speaker section contains the eight voice coils that are placed on the same core. The diameter of the diaphragm is 25.5 cm. In addition to the DSM, a second-order mismatch shaper circuit is programmed in the FPGA. The CMOS buffer is implemented along with inverters. The photograph of the prototype system, excluding the loudspeaker subunits, is shown in Fig.13.

The output fluxes of the voice coils are combined and original signal is reproduced. Furthermore, since the output signal is an ON-OFF signal, it is possible to amplify it using the buffer.

The effectiveness of the proposed speaker system is tested by a prototype system. The test system is shown in Fig.14. In this experiment, a 16-bit 1-kHz sine wave

is inputted to the FPGA board. In the output stage, a sound wave is outputted from the eight voice coils.

The measured output spectrum of the prototype system is shown in Fig.15. The THD and SPL of the digital speaker are 0.1% and 104 dB, respectively.

The frequency response is shown in Fig.16. The fundamental frequency response is determined by the frequency response of a speaker, which is has the same structure as the conventional loudspeaker unit.

The proposed system has several merits, which are stated as follows:

- The loudspeaker subunits can be digitally driven.
- Since the loudspeaker subunits are driven by the ON-OFF signal, the power efficiency is high.
- Since the loudspeaker subunits are driven by the ON-OFF signal, the effect of the nonlinearity in the loudspeaker subunits can be reduced.
- A thin speaker system can be realized by using the dynamic speaker (when a piezoelectric speaker is the loudspeaker subunits).

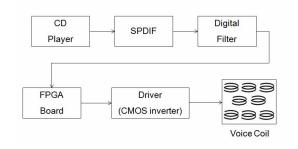


Figure 12: Block diagram of prototype digital speaker.



Figure 13: Photograph of prototype board.

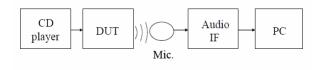


Figure 14: Block diagram of measurement system.

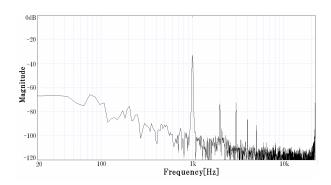


Figure 15: Output spectrum of Digital-SP

(input: 1-kHz sine wave).

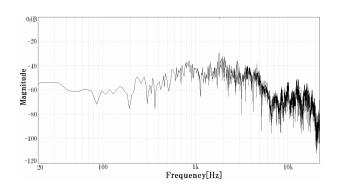


Figure 16: Output spectrum of Digital speaker (input: white noise).

- The out-of-band noise caused by the DSM can be reduced by using the multibit DSM.
- The sound pressure can be increased by using several loudspeaker subunits.
- It is flexible unlike the conventional speaker; new applications such as its attachment on a sheet of paper are possible in the future.

5. CONCLUSION

A novel dynamic Digital-SP system, which has eight voice coils and is directly driven by digital signals, has been proposed. The effectiveness of the proposed Digital-SP has been confirmed by the measured data of the prototype Digital-SP. An output power of 2.3 W and THD of 0.1% have been obtained by using a 1.5-V battery without a DC-DC converter. The SPL was 104 dB. A digital speaker system for high fidelity audio can be realized by using the proposed method.

6. ACKNOWLEDGEMENT

This work was supported by a Grant-in-Aid for Scientific Research.

7. REFERENCES

- [1] H. Ueno, T. Soga, K. Ogata, A Yasuda, "Digital-driven piezoelectric speaker using multi-bit delta-sigma modulation," presented at the AES 121st Convention, 2006 October 5.
- [2] M. J. Story, "Digital to analog converter adapted to select input sources based on a preselected algorithm once per cycle of a sampling signal," U.S. Patent 5 138 317, 1992 August 11.
- [3] B. H. Leung, "Architectures for multibit oversampled A/D converter employing dynamic element matching techniques," in Proc. IEEE ISCAS, pp. 1657-1660 (1991).
- [4] R. T. Baird, T. S. Fiez, "Linearity enhancement of multibit Delta-sigma A/D and D/A converters using data weighted averaging," IEEE J. Solid-State Circuits, vol. 42, pp. 753-762 (1995 December).

[5] A. Yasuda, H. Tanimoto, T. Iida, "A Third-order modulator using second-order noise-shaping dynamic element matching," IEEE J. Solid-State Circuits, vol. 33, pp. 1879-1886 (1998 December).