a module solution provider

WG7351-00 WLAN/BT/FM Module

TI WL1273L IEEE 802.11a/b/g/n

BT4.0 & FM solution

Datasheet

Revision 0.2

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1. OVERVIEW

WG7351, a WiFi , Bluetooth and FM SiP (system in package) module, is the most demanded design for all handset and portable devices with TI WL1273L IEEE 802.11a/b/g/n and BT4.0 solutions to provide the best WiFi and BT coexistence interoperability and power saving technologies from TI.

1.1. General Features

- WLAN, Bluetooth and FM radio on a SiP module
- LGA69 pin package
- Dimension 11.6mm(L) x 9.6mm(W) x 1.4mm(H)
- Based on TI WL1273L 65-nm CMOS technology packaged in WSP for module
- Seamless integration with TI OMAP application processor and GSM-GPRS-UMTS chipset
- Internal support for WLAN and Bluetooth Co-existence (bandwidth sharing, antenna sharing)
- Direct connection to battery using external switching mode power supply supporting 4.8V to 2.7V operation
- VIO in the 1.8V domain
- Fast Clock using external TCXO crystal

2. FUNCTIONAL FEATURES

2.1. Module Block Diagram
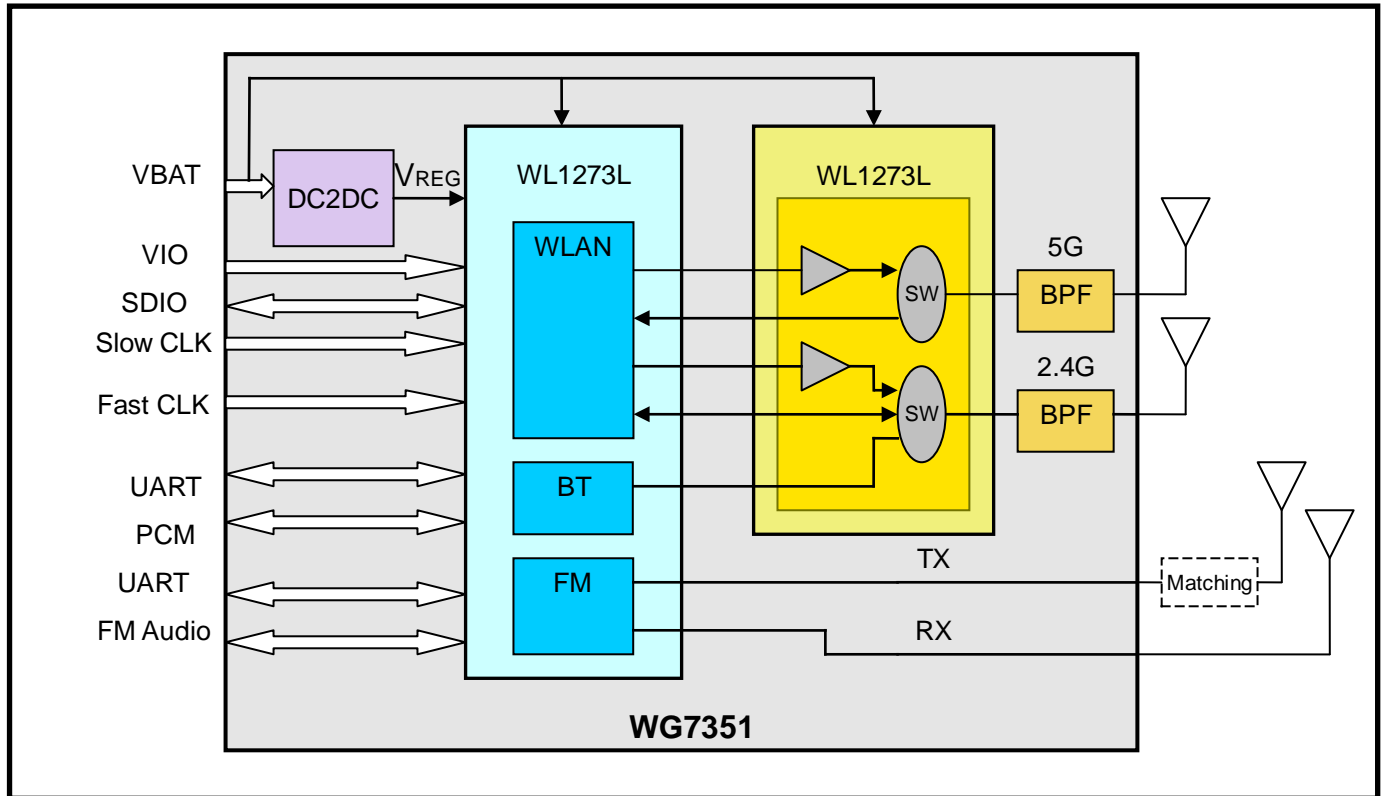
2.2. Block Functional Feature

2.2.1. WLAN Features

- Support 802.11 2.4GHz b/g/n mode
- Support 802.11 5GHz a/n mode
- Optimized for ultra low current consumption in all operating modes including extremely low power modes
- IEEE Std 802.11d, e, h, I, k, r, s PICS compliant
- Supports Cisco Client eXtensions (CCX) standard
- Support Secure Digital Input/Output (SDIO) Interfaces
- Medium-Access Controller (MAC)

- Embedded ARM Central Processing Unit (CPU)
- 292kByte (Used for Program code, data and packet data) Embedded Random-Access Memory (RAM)
- Hardware-Based Encryption/Decryption Using 64-, 128-, and 256-Bit WEP, TKIP or AES Keys
- Supports Wi-Fi Protected Access (WPA and WPA2.0) and IEEE Std 802.11i [Includes Hardware-Accelerated Advanced-Encryption Standard (AES)]
- Designed to Work with IEEE Std 802.1x for Virtual Private Network (VPN) Solutions

- Baseband Processor
  - All IEEE Std 802.11a/b/g and 802.11n Data Rates up to 72.2Mbps
- 2.4 GHz Radio
  - Digital Radio Processor (DRP) implementation
  - Internal LNA
  - Supports: IEEE Std 802.11b, 802.11g, 802.11b/g, 802.11a and 802.11n

2.2.2. Bluetooth Features

- Bluetooth 1.1, 1.2, 2.0+EDR and 2.1+EDR, 3.0 and 4.0 specification compliant – up to HCI level
- BT Enhanced Data Rate (2 and 3 Mbps)
- Enhanced host Interfaces (UART)
- Very low power consumption
- On-chip Embedded radio
- Embedded ARM Microprocessor System
- Temperature detection and compensation mechanism ensure minimal variation in the RF performance over the entire temperature range
- A2DP support
- Wide-Band Speech support

2.2.3. BLE Features

Fully compliant with BT4.0 Low Energy (BLE) dual mode standard:
- TI BLE solution optimized for the proximity/sports use-case
- Supports large number of multiple connections (up to 10)
- Multiple sniff instance are tightly coupled to achieve minimum power consumption
- Independent buffering for LE allows having large number of multiple connections without affecting BR/EDR performance
- Includes built-in coexistence and prioritization handling for BT, BLE and WLAN

Notes: Advanced audio and voice processing (AVPR) capabilities, and ANT are not available when BLE is enabled.

2.2.4. ANT Features

Fully compliant with all ANT Protocols:
- ANT solution optimized for the fitness, health and consumers use-case
- Supports large number of multiple connections (up to 8)
- Simple to complex network topologies
- Support high-resolution proximity pairing
- Includes built-in coexistence and prioritization handling for BT, BLE and WLAN
- ANT provides immediate access to the millions of ANT+ sensors already in the market and an ongoing option for cost and power optimized sensors

The ANT protocol has been designed to very power-efficient, yet is flexible enough to support various network topologies (point-to-point, star, 1-to-N, N-to-1) and data transfer modes (broadcast, broadcast with acknowledge, mass data transfer). Each logical ANT channel can be independently configured for 1-way or 2-way operation.

Notes: Advanced audio and voice processing (AVPR) capabilities, and BLE are not available when ANT is enabled.

2.2.5. FM Radio (RX/TX) Features

- On-Chip FM Receive
- On-Chip 0dBm output FM Transmitter
- Operation through BT host interface (UART) or separate I^2C interface for control and RDS data transfer
- Up to 48k Samples/sec audio sampling for stereo headsets
- Frequency resolution: 50-kHz step tuner
- Compatibility with Europe/US (87.5-108MHz) and Japan (76-90 MHz) FM Bands
- Full digital implementation
- Digital MPX signal, thus eliminating need for noise blanking circuits
- Integrated RDS/RDBS features
- Soft Mute
- Stereo/Mono blend based on signal condition for RX
- Selectable 50/75-us de-emphasis filter
- I^2S format for stereo/mono digital audio data
- Analog stereo audio inputs/outputs
- Software selectable level for soft mute and stereo/mono blend level for RX
- Fast independent up/down tuning function
- Supports a dedicated enable pin for the FM IP

3. MODULE SPECIFICATION

3.1. Absolute Maximum Ratings

Over operating free-air temperature range

Characteristics		Value	Unit
Supply Voltage Range	VBAT	-0.5 to 5.5	V
	VIO	-0.5 to 2.1	V
Input Voltage to Analog Pins		-0.5 to 2.1	V
Input Voltage to all Other Pins		-0.5 to VIO + 0.5V	V
Operating Ambient Temperature Range		-20 to 70	˚C
Storage Temperature Range		-40 to 85	˚C

3.2. Recommended Operating Conditions

The WG7351 requires three two supplies: VBAT and VIO.

Power Supply	Voltage		
	Min.	Typ.	Max.
VBAT	2.7V	3.3V	4.8V
VIO	1.62V	1.8V	1.92V

3.3. WLAN RF Characteristic

3.3.1. 2.4-GHz Receiver

CHARACTERISTICS	CONDITION	SYMBOL	MIN	TYP	MAX	UNIT
Operation frequency range			2412		2484	MHz
Sensitivity	1 Mbps DSSS		-92.5	-96.0	–	dBm
	2 Mbps DSSS		-90.0	-93.5	–	
	5.5 Mbps CCK		-88.0	-91.0	–	
	11 Mbps CCK(1)		-85.0	-87.0	–	

	6 Mbps OFDM		-88.0	-90.0	–	
	9 Mbps OFDM		-87.5	-89.5	–	
	12 Mbps OFDM(2)		-86.0	-88.0	–	
	18 Mbps OFDM		-84.5	-86.5	–	
	24 Mbps OFDM		-82.0	-83.5	–	
	36 Mbps OFDM		-79.0	-80.0	–	
	48 Mbps OFDM		-74.5	-76.0	–	
	54 Mbps OFDM(3)		-70.0	-74.0	–	
	MCS0(4)		-87.5(5)	-90.0	–	
	MCS7(4)		-68.0(5)	-71.0	–	
Max Iput Level(6)	OFDM(11g or 11n)				-15	dBm
	CCK				-8	
Adjacent Channel Rejection	54OFDM	ADJCI	30			dB
	11CCK		46.5			
LO Leakage					-70	dBm

(1) For channel 14, sensitivity is degraded up to 1.5 dB in 802.11b/g/n.

(2) For channel 13 and 14, sensitivity is degraded up to 1 dB in 802.11g/n.

(3) For channel 13 and 14, sensitivity is degraded up to 1.5 dB in 802.11g/n.

(4) For channel 13 and 14, sensitivity is degraded up to 2 dB in 802.11g/n.

(5) Greenfield mode : degrade 1 dB for mixed mode

3.3.2. 5-GHz Receiver

CHARACTERISTICS	CONDITION	SYMBOL	MIN	TYP	MAX	UNIT
Operation frequency range		F_{REF}	4900		5825	MHz
Sensitivity	MCS0		-84.5	-86.5	–	dBm
	MCS7		-65.0(1)	-68.0	–	
	54 Mbps OFDM(3)		-68.0(1)	-71.0	–	
	48 Mbps OFDM		-70.5	-73.5	–	
	36 Mbps OFDM		-74.5	-77.5	–	
	24 Mbps OFDM		-77.5(1)	-80.5	–	
	18 Mbps OFDM		-80.5	-83.5	–	
	12 Mbps OFDM(2)		-82.5(1)	-85.5	–	

	9 Mbps OFDM		-84.0	-87.0	–	
	6 Mbps OFDM		-85.0	-88.0	–	
Max Input Level	OFDM				-17	dBm
Adjacent Channel Rejection	54M OFDM	ADJCI	17			dB
LO Leakage					-63	dBm

(1) Up to 1-dB degradation in 5852 with F_{REF} = 26MHz

3.3.3. 2.4-GHz Transmitter

CHARACTERISTICS	CONDITION	SYMBOL	MIN	TYP	MAX	UNIT
Maximum RMS output power	1 Mbps,2 Mbps		17.0	18.0	–	dBm
	5.5 Mbps,11 Mbps		16.5	17.5	–	
	6 Mbps, 9 Mbps		16.5	17.5	–	
	12 Mbps,18Mbps		16.0	17.0	–	
	24 Mbps,36 Mbps		14.0	15.5	–	
	48 Mbps,54 Mbps		12.5	14.0	–	
	MCS7(Greenfield)		11.5	13.0	–	
Special mask margin	Each frequency region detailed in(1)		2			dB
EVM	24 Mbps and 36 Mbps at +14.0dBm		-23			dB
	48 Mbps and 54 Mbps at +12.5dBm) (2)		-25			
	MCS7 at + 11.5dBm (2)		-28			
In band power variation			+/-1			dB

(1) Spectral mask regions are defined according to the IEEE802.11 specifications (Regions A through

   C for 802.11b;Regions D through F for 802.11g):

   Region A: f∈[Fc-22MHz,Fc -11 MHz] □ [Fc+11 MHz, Fc +22 MHz]

   Region B: f∉ [Fc-22MHz,Fc +22 MHz]

   Region C: f∈[Fc-11MHz,Fc -9 MHz] ∪ [Fc+9 MHz, Fc +11 MHz]

   Region D: f∈[Fc-20MHz,Fc -11 MHz] ∪ [Fc+11 MHz, Fc +20 MHz]

   Region E: f∈[Fc-30MHz,Fc -20 MHz] ∪ [Fc+20 MHz, Fc +30 MHz]

   Region F: f∉ [Fc-30MHz,Fc +30 MHz]

(2) For operation at temperature below -30℃ EVM may degrade by up to 1dB.

3.3.4. 5-GHz Transmitter

CHARACTERISTICS	CONDITION	SYMBOL	MIN	TYP	MAX	UNIT
Maximum RMS output power	6 Mbps,9 Mbps		16.5	18.0	–	dBm
	12 Mbps,18Mbps		14.5	16.0	–	
	24 Mbps,36 Mbps		13.5	15.0	–	
	48 Mbps,54 Mbps		12.0	13.5	–	
	MCS7(Greenfield)		11.0	12.5	–	
Special mask margin	Each frequency region detailed in		2			dB
EVM	24 Mbps and 36 Mbps at +13.5dBm		-23			dB
	48 Mbps and 54 Mbps at +12.0dBm		-25			
	MCS7 at + 11.0dBm		-28			
In band power variation			+/-1			dB

3.4. Bluetooth RF

3.4.1. BT Transmitter, GFSK, Class 2 & Class 1.5

Characteristics		Min	Typ	Max	Unit
RF output power	VDD_LDO_IN_CLASS1P5 = VBAT	7	9	---	dBm
	VDD_LDO_IN_CLASS1P5 = 1.8V	4	7	---	
Power variation over BT band		-1		1	dB
Gain control range			30		dB
Power control step		2	5	8	dB

3.4.2. BT Receiver Characteristics, In-Band Signals

Characteristics		Min	Typ	Max	Unit
Sensitivity	GFSK, BER = 0.1%	-88	-90		dBm
	Pi/4-DQPSK, BER = 0.01%	-88	-90		
	8DPSK, BER = 0.01%	-82	-84		
Max. useable input power	GFSK, BER = 0.1%	-5			dBm
	Pi/4-DQPSK, BER = 0.1%	-10			
	8DPSK, BER = 0.1%	-10			

3.5. BLE RF

BT Transmitter						
Characteristics		Min	Typ	Max	BLE SPEC	Unit
RF output power	CLASS1P5 = VBAT	7	9	---	<= 10	dBm
Power variation over BLE band		-1		1		dB

BT Receiver Characteristics, In-Band Signals						
Characteristics		Min	Typ	Max	BLE SPEC	Unit
Sensitivity	PER=30.8%	-89	-92	---	<= -70	dBm
Max. useable input power	GFSK, PER = 30.8%	-5	---	---	>= -10	dBm

3.6. FM Radio Electrical Characteristics

Characteristics	Condition	Min	Typ	Max	Unit
Audio output impedance	FM function enabled and during auto-search			50	Ω
	FM function disabled and when muted	50			KΩ
Audio input impedance		30			KΩ
Selectable RF Rx input	With external matching circuitry –		50	500	Ω

impedance	Default = 50 Ω				
RF input return loss	With external matching circuitry	-10			dB
Receiver current consumption	FM Rx at sensitivity level, BT in deep sleep		12	15	mA
Transmitter current consumption	FM TX on, BT in deep sleep · Digital audio / Analog audio		13	16	mA
FM off current			1	2	uA

3.7. External Slow Clock Input (SLEEP_CLK)

The external slow clock input SLEEP_CLK must be present at all times. The slow clock is used to maintain timers that synchronize the device to the access point (AP) beacons.

Table 1. External Slow Clock Input Requirements

Characteristics[1]	Condition	Sym	Min	Typ	Max	Unit
Input slow clock frequency				32768		Hz
Input slow clock accuracy	WLAN, BT, FM_RX				± 150	ppm
	FM_TX[2]				±40	
Input transition time T_r/T_f -10% to 90%		Tr/Tf			100	ns
Frequency input duty cycle			15	50	85	%
Input voltage limits	Square wave, DC-coupled	V_{IH}	0.65 × VDDS		VDDS	V_{peak}
		V_{IL}	0		0.35 × VDDS	
Input impedance			1			MΩ
Input capacitance					5	pF
Rise and fall time					100	ns
Phase noise[3]	1kHz				−125	dBc/Hz
Jitter[3]	Integrated over 300Hz - 15000Hz				1	Hz

(1) Slow clock is a fail safe input
(2) If the available slow clock source does not meet the ±40 ppm requirement, there are two options;
  • Use the fast clock for the FM_TX functionality. This is configured using a vendor-specific command to switch to Fref operation after enabling the FM core with the slow clock source.
  • Enable clock error calibration in the FM core to compensate for the clock source error. The calibration can be done using a known vendor-input clock error or intrinsically to the core (self-calibration).
(3) Not required if fast clock is used for FM TX and RX.

3.8. External Fast Clock Input

3.8.1. Reference Clock

WG7351 supports the following reference clocks: 19.2, 26, 38.4 and 52MHz. The supported sources for the reference clock are:
● Analog sine wave (AC coupled)
● Digital clock, VDDS level

3.8.2. External Digital Fast Clock Source

3.8.1. External Digital Fast Clock Source

Clock input level = 500 mVp-p typical (Sinusoidal)
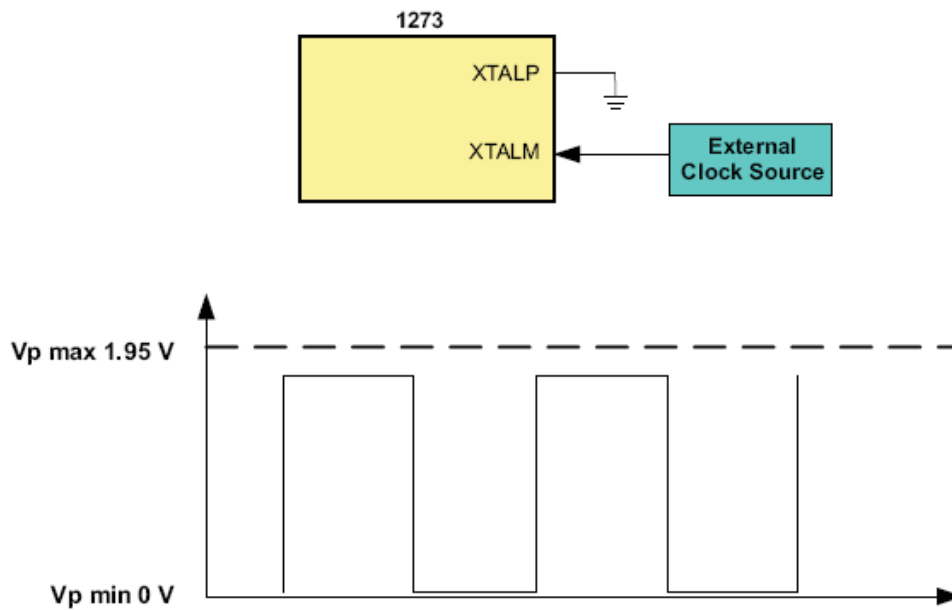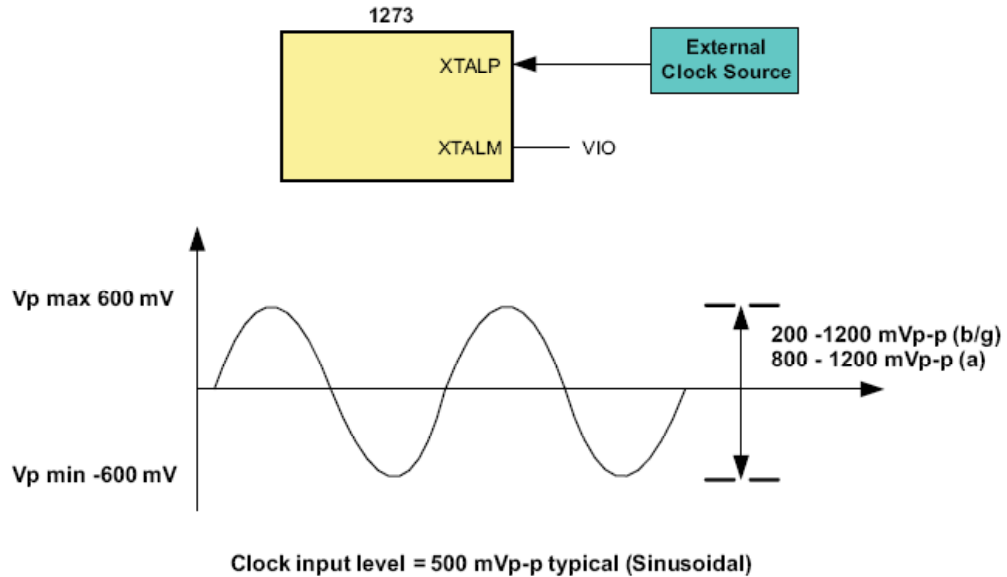
In cases where the input amplitude is greater than 1.2V, the amplitude should be lowered by reducing the value of the coupling capacitor, or by using a resistor to ground. This forms a voltage divider capacitance to provide the required at the module input.

Table 2. External Fast Clock Input Requirements

Characteristics [1] [2]	Condition		Sym	Min	Typ	Max				Unit
Supported frequencies			F_{ref}	19.2, 26, 38.4, 52						MHz
Reference frequency accuracy	Initial + temp + aging					±20				ppm
Clock input voltage limits	AC coupled (sine wave)			800		1200				mV $_{p-p}$
	Digital			0		V_{IO}				V
Duty cycle				35	50	65				%
Sine wave clock harmonics	2nd Harmonic					−30				dBc
	3rd Harmonic					−14				
	4th Harmonic					−30				
Rise / Fall times	Square-wave clock		T_r/T_f			10				% of clock period
Settling time	Time from asserting CLK_REQ/CLKREQ_n until Clock is available at device input					20	20	20	20	ms
Phase noise	FM, BT, WLAN b/g/n modes (200 mVp-p min amplitude)	offset				19.2MHz	26MHz	38.4MHz	52MHz	dBc/Hz
		1kHz				−126	−123.4	−120	−117.3	
		10kHz				−136	−133.4	−130	−127.3	
		100kHz				−141	−138.4	−135	−132.3	
	WLAN a mode (800 mVp-p min amplitude)	1kHz				−132	−129.4	−126	−123.4	
		10kHz				−145	−142.4	−139	−136.4	
		100kHz				−150	−147.4	−144	−141.4	

(1) The slope of the clock at zero-crossings should not be less than that of a 200 mV$_{p-p}$ sine-wave (800 mV$_{p-p}$ for 11a band).
(2) System clock is a fail safe input

4. POWER CONSUMPTION

4.1. Device Shutdown Current

The SDIO/CLK_REQ lines should be driven by the host to prevent leakage in sleep/shutdown modes.

MODE DESCRIPTION	POWER SUPPLY	TYP	MAX	UNIT
Shutdown mode (BT, WLAN and FM sections in shutdown mode) Values are over process and at room temperature	V_{REG} 1.8V	2	3	μA
	1.8V (VIO)	6.5	7.5	
	Total V_{BAT} at 3.6V	14	26	

4.2. WLAN Power Consumption

WLAN supply current was measured using the HDK and the TrioScope tool, over process and temperature at F_{ref} 38.4MHz unless otherwise specified.

4.2.1. Active Mode

- During Listen Mode operation, the radio is in a low power mode optimized to receive only 11b beacons. The DC2DC, FEM and WL1273L devices are active but consume less current.
- In STBY mode, no RF operation required. The DC2DC, FEM and WL1273L device are active but consume lower current.
- In TX and RX modes, all devices are active and consume maximum currents.

MODE DESCRIPTION		POWER SUPPLY		11Mbps IEEE802.11b		54/65Mbps IEEE802.11g/n		54/65Mbps IEEE802.11a/n		UNIT
				TYP[1]	MAX[2]	TYP[1]	MAX[2]	TYP[1]	MAX[2]	
Transmit data	IEEE802.11b/g: Packet size = 2048 bytes IEEE802.11n: Packet size = 1024 bytes IEEE802.11b, delay = 0.004ms IEEE802.11g/n delay = 0.002ms	V_{REG} 1.8V		139	156	139	156	150/165	175/185	mA
		1.8V (VIO)		0.26	0.3	0.26	0.3	0.26	0.3	
		Total V_{BAT} = 3.6V	FEM current only	195	214	113	122	150	185	
			System current	270	292	195	207	235	271	
Receive data[3]		V_{REG} 1.8V		156	168	156	168	165	183	mA
		1.8V (VIO)		0.23	0.3	0.23	0.3	0.23	0.3	
		Total V_{BAT} = 3.6V		96	105	96	105	98	107	
Listen[3]		V_{REG} 1.8V		113	123	n/a	n/a	n/a	n/a	mA
		1.8V (VIO)		0.23	0.3	n/a	n/a	n/a	n/a	
		Total V_{BAT} = 3.6V		68	74	n/a	n/a	n/a	n/a	
STBY		V_{REG} 1.8V		8.5	20	8.5	20	8.5	20	mA
		1.8V (VIO)		0.23	0.3	0.23	0.3	0.23	0.3	
		Total V_{BAT} = 3.6V		6	9	6	9	6	9	

[1]   Nominal process at 25°C
[2]   Over process and temperature
[3]   Channel 14 values add up to 2mA

4.2.2. Inactive and Dynamic Modes

MODE DESCRIPTION	POWER SUPPLY	TYP	MAX	UNIT
Sleep mode (BT and FM in reset)[1][2]	V_{REG} 1.8V	60	92	
	1.8V (VIO)	11	17	μA
	Total V_{BAT} at 3.6V	96	109	

[1]   Values indicate current between beacons
[2]   Room temp over process

MODE DESCRIPTION[1]	POWER SUPPLY	MAX	UNIT
Dynamic mode Beacon (DTIM=1 ; TBTT = 100ms; Beacon duration ~1.6ms ; Rate=1Mbps) Beacon in Listen mode	Total V_{BAT} at 3.6V to TPS62611	0.82	mA

[1]   This mode reflects results with software drivers and not the Trioscope tool.

4.3. BT Power Consumption

BT supply current was measured using the HDK and HCI Tester tool at F_{ref} 38.4MHz.

4.3.1. Static State

CHARACTERISTICS		TYP[1]	MAX[2]	UNIT
Supply current in deep sleep mode	V_{REG} 1.8V	41	63	µA
	VIO	12	15	
	V_{BAT}	62	80	

[1]   Room temperature, nominal
[2]   Room temperature, over process

4.3.2. Dynamic State

Transmit power at 4dBm, nominal, room temperature, V_{BAT}=3.6V, F_{ref} at 38.4MHz.

USE CASE	MODE DESCRIPTION	FULL V_{BAT} SOURCE (using DC2DC)	MIXED MODE		FULL 1.8V SOURCE (no DC2DC)	UNIT
			1.8V[1]	V_{BAT}[2]		
Idle current (ARM off)[3]	Master/Slave	1.8	2.9	0	2.9	mA
SCO link HV3	Master/Slave	8	11.4	1.2	12.9	
eSCO link EV3 64Kbps, no retransmission	Master/Slave	8.2	11.5	1.3	13.2	
eSCO link 2-EV3 64Kbps, no retransmission	Master/Slave	5.6	8.5	0.6	9.5	
GFSK full throughput: TX=DH1, RX=DH5	Master/Slave	23.5	37.5	1.2	38.9	
EDR full throughput: Tx=2-DH1, RX=2-DH5	Master/Slave	24.3	38.6	1.1	40.3	
EDR full throughput: Tx=3-DH1, RX=3-DH5	Master/Slave	24.9	38.5	1.1	40.5	
Sniff, 1 attempt, 1.28sec	Master/Slave	100/110	90/115	<10	95/125	µA
Page or Inquiry Scan 1.28s, 11.25ms	Master/Slave	230	315	0	315	
Page scan 1.28s, 11.25msec and Inquiry Scan 2.56s, 11.25ms	Master/Slave	320	435	0	435	
Low power scan, 1.28s interval	Master/Slave	145	150	0	150	

[1]   Voltage input at INPUT_VBAT_SUPPLY
[2]   Voltage input at BT_CLASS_1P5
[3]   IDLE is a state in which the BT is awake and communicates with the host, but there is no RF activity.

4.4. BLE Power Consumption

BLE supply current was measured using the HDK and HCI Tester tool at Fref = 38.4 MHz.

Operational Mode	Description	Full V_{BAT} Source	Unit
Advertising (non-connectable)	AdvInterval = 1.28 s Adv Data = 15 Octets	1124	uA

	TX output power = +10 dBm Advertising on 3 adv channels	
Advertising (discoverable)	AdvInterval = 1.28 s Adv Data = 15 Octets TX output power = +10 dBm Advertising on 3 adv channels	135
Scanning	scanInterval = 1.28 s scanWindow = 11.25 ms Listens on single frequency per window	245
Link Layer connection (master)	Master role connInterval = 500 ms connSlaveLatency = 0 Empty TX/RX LL packets TX output power = +10 dBm	160

5. Module Pin Assignment

5.1. Module Pin Location
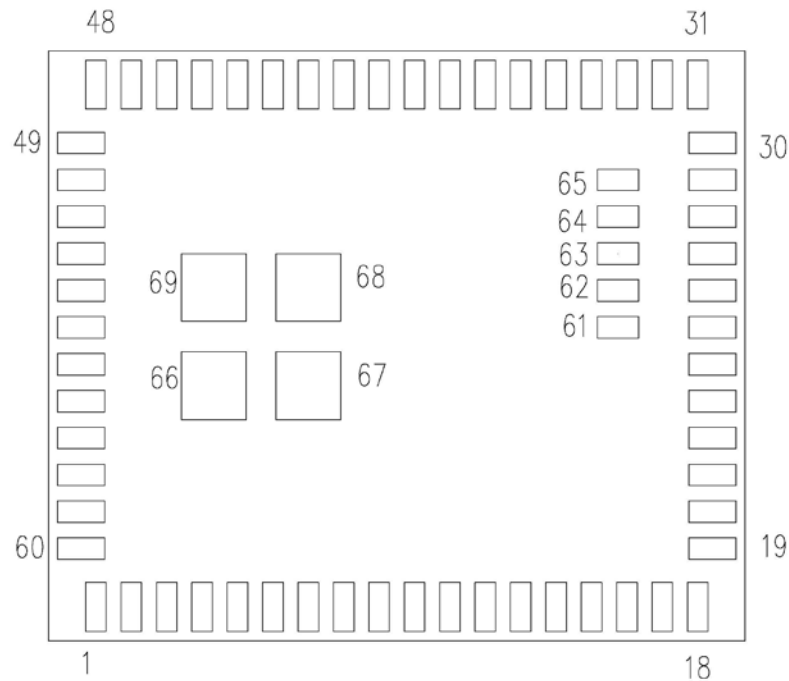
Top View (Perspective view)

5.2. Pin Out Description

Pin No.	Name	Type	System	Description
1	GND	GND	-	GROUND
2	5G-ANT	I/O	WLAN	RF transmitter output and RF receive input
3	GND	GND	-	GROUND
4	HOST_WAKE	I/O	BT	Host Wake
5	CLK_REQ	I/O	-	Clock Request
6	GND	GND	-	GROUND
7	1V8_PRE_REG	P	-	Monitor pin for feedback voltage from DCDC converter

8	VDD_LDO_IN_CLASS1P5	P	-	For choosing BT operation mode.
9	VBAT	P	-	Power supply input
10	VIO	P	-	Power supply input
11	GND	GND	-	GROUND
12	BT_RESETX	I	BT	BT_RST
13	WLAN_IRQ	O	WLAN	WLAN interrupt request
14	FM_EN	I	FM	FM_RST
15	WL_RS232_TX	I/O	WLAN	RS232_TX or I2C_M_SDA
16	WL_RS232_RX	I/O	WLAN	RS232_RX or I2C_M_SCL
17	WLANENABLE	I	WLAN	WL_RST
18	GND	GND	-	GROUND
19	SDIO_D2	I/O	WLAN	SDIO: Data2
20	SDIO_D1	I/O	WLAN	SDIO: Data1
21	SDIO_D3	I/O	WLAN	SDIO: Data3
22	SDIO_CMD	I/O	WLAN	SDIO: CMD
23	SDIO_CLK	I/O	WLAN	SDIO: CLK
24	SDIO_D0	I/O	WLAN	SDIO: Data0
25	GND	GND		GROUND
26	SLEEP_CLK	I	WLAN	Sleep Clock Input
27	GND	GND		GROUND
28	FM_TX_ANT	O	FM	FM TX Antenna
29	GND	GND		GROUND
30	FM_RX_ANT	I	FM	FM RX Antenna
31	GND	GND		GROUND
32	GND	GND		GROUND
33	FM_AUD_IN_R	I	FM	FM Audio Input
34	FM_AUD_IN_L	I	FM	FM Audio Input
35	FM_AUD_OUT_R	O	FM	FM Audio Output
36	FM_AUD_OUT_L	O	FM	FM Audio Output
37	GND	GND		GROUND
38	XTALP	-		FREF Input
39	XTALM	-		FREF Input
40	GND	GND		GROUND
41	BT_WAKEUP	I/O	BT	BT_WU I/F or BT DC2DC or BT_IRQ
42	UART_RX	I/O	BT	BT_UART I/F

43	UART_RTS	I/O	BT	BT_UART I/F
44	UART_TX	I/O	BT	BT_UART I/F
45	UART_CTS	I/O	BT	BT_UART I/F
46	GND	GND		GROUND
47	2.4G_ANT	I/O	BT/WLAN	RF transmitter output and RF receive input
48	GND	GND		GROUND
49	GND	GND		GROUND
50	GND	GND		GROUND
51	PCM_SYNC	I/O	BT	PCM I/F
52	PCM_CLK	I/O	BT	PCM I/F
53	PCM_OUT	I/O	BT	PCM I/F
54	PCM_IN	I/O	BT	PCM I/F
55	FM_I2S_DO	I/O	FM	FM I2S I/F
56	FM_I2S_DI	I/O	FM	FM I2S I/F
57	FM_I2S_FSYNC	I/O	FM	FM I2S I/F
58	FM_I2S_CLK	I/O	FM	FM I2S I/F
59	GND	GND	-	GROUND
60	GND	GND	-	GROUND
61	FM_SCL	I/O	FM	FM I2C IF
62	FM_IRQ	I/O	FM	FM I2C IF
63	FM_SDA	I/O	FM	FM I2C IF
64	BT_UART_DBG	I/O	BT	BT_UART_DBG
65	UART_DBG	I/O	WLAN	WLAN_UART_DBG
66	GND	GND		GROUND
67	GND	GND		GROUND
68	GND	GND		GROUND
69	GND	GND		GROUND

6. Power Sequence

6.1. WLAN Power on Sequence
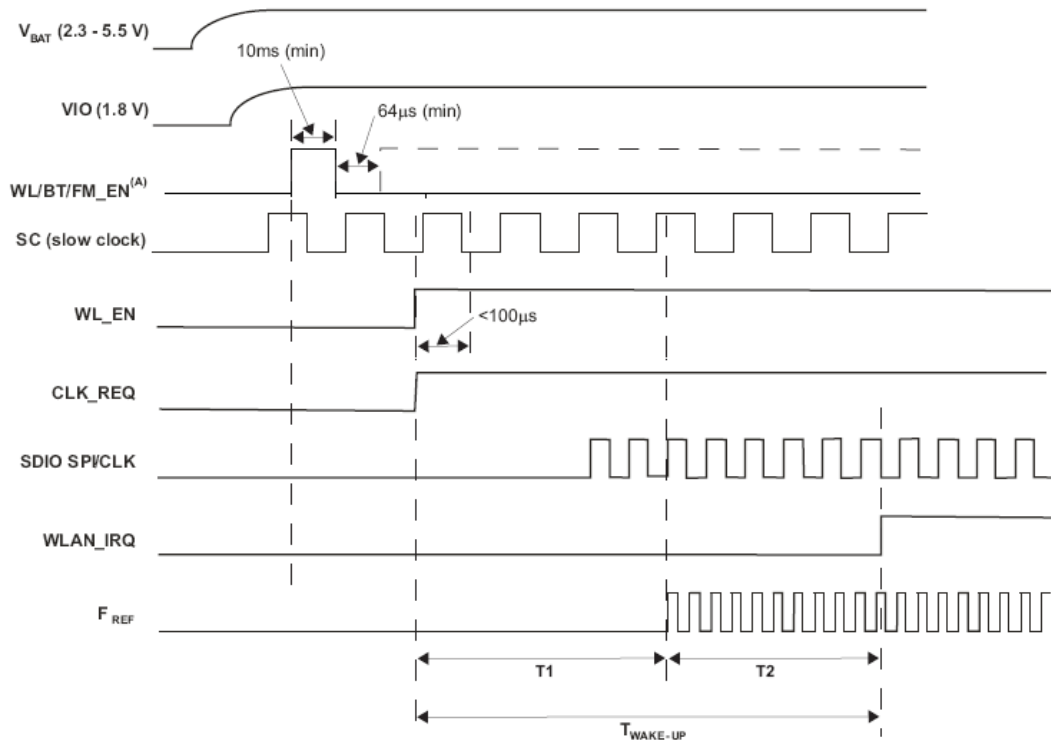
WLAN Power on sequence

The following sequence describes device power up from shutdown. Only the WLAN Core is enabled; the BT and FM cores are disabled.

VBAT, VIO and SLOWCLK must be available before WL_EN.

The duration of T1 is defined as the time from WL_EN=high until Fref is valid for the SoC.
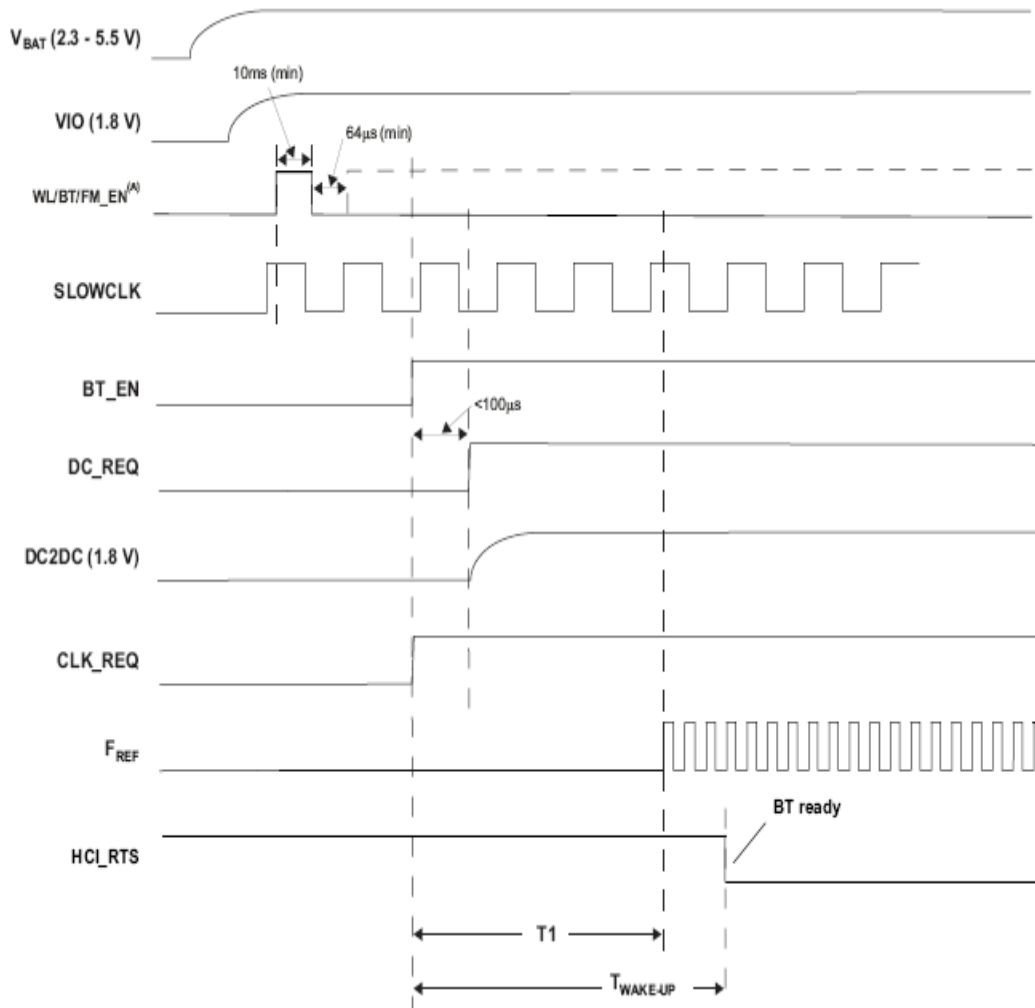
T1 ~ 55ms

The duration of T2 depends on:

- Operation system
- Host enumeration for the SDIO
- PLL configuration
- Firmware download

- Releasing the core from reset
- Firmware initialization

6.2. Bluetooth Power Up/Down Sequence

Power up requirements:
1. BT_EN must be low
2. VIO must be stable before releasing BT_EN.
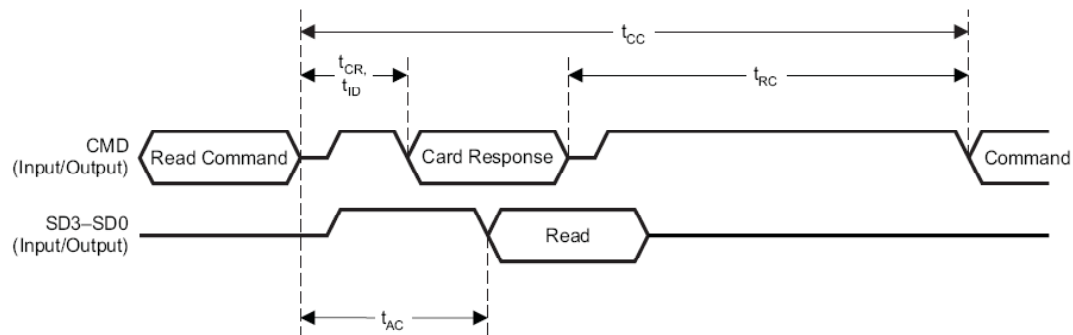3. Slow clock must be stable within 2 ms of BT_EN high.

Bluetooth Power Up/Down sequence

WG7351 indicates completion of power up sequence by asserting RTS low. This occurs up to 100ms after BT_EN goes high.

7. Interface Characteristics

## 7.1. WLAN SDIO Characteristic

7.1.1. SDIO Read Timing

SDIO Single Block Read

Table 3. SDIO Read Switching characteristics

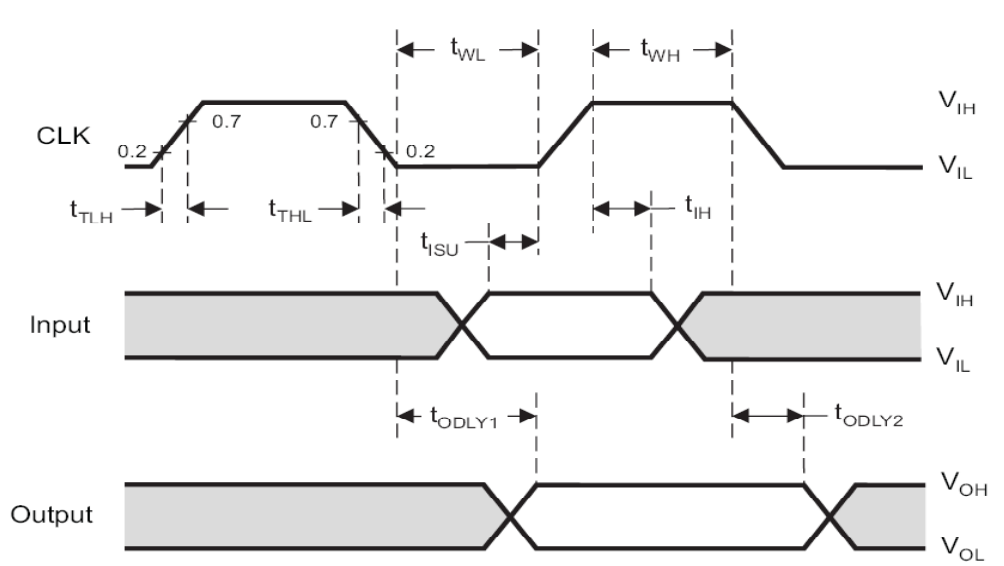| Parameter		Min.	Max.	Unit
t_{CR}	Delay time, assign relative address/data transfer mode, CMD command invalid to CMD response valid	2	64	Clock Cycles
t_{ID}	Delay time, identification, CMD command invalid to CMD response valid	5	5	
t_{CC}	Delay time, CMD command invalid to CMD response valid	8	---	Clock Cycles
t_{RC}	Delay time, CMD response invalid to CMD command valid	8	---	Clock Cycles
t_{AC}	Access time, CMD command invalid to SD3-SD3 read data valid	2	---	Clock Cycles

7.1.2. SDIO Interface Write Timing
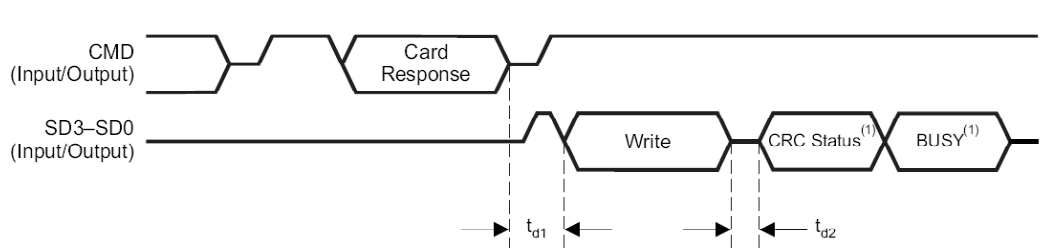
(1) CRC status and busy waveforms are only for data line 0. Data lines 1-3 are N/A. The busy waveform is optional and may not be present.

SDIO Single Block Write

Table 4. SDIO Write Switching characteristics

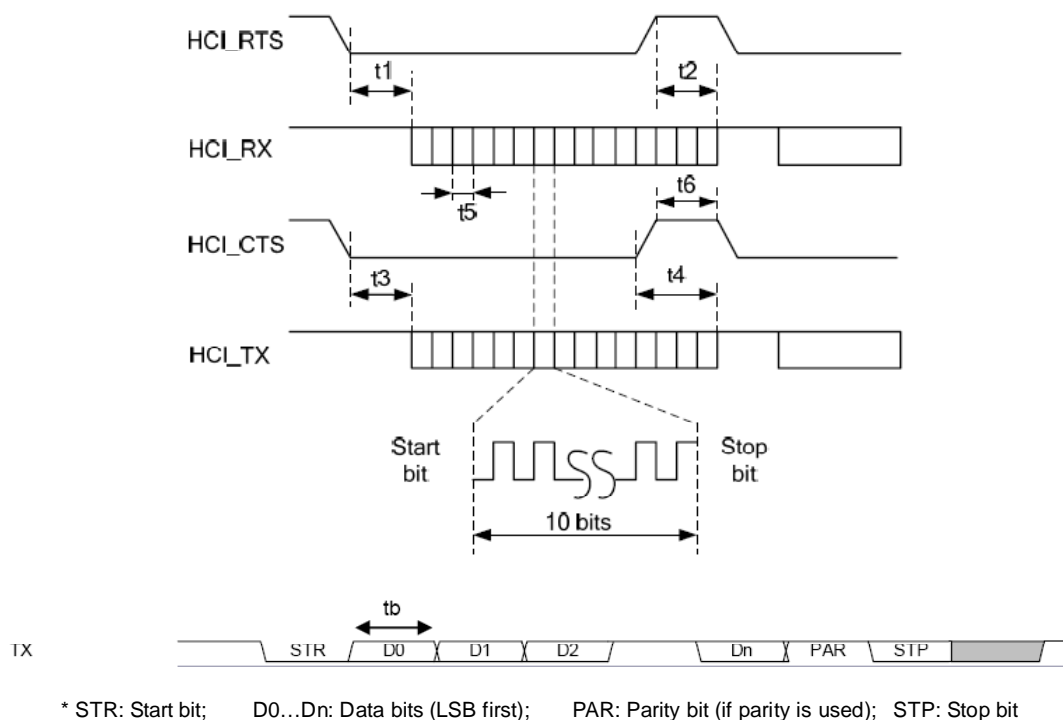|	Parameter	Min.	Max.	Unit
t_{d1}	Delay time, CMD card response invalid to SD3-SD0 write data valid	2	---	Clock Cycles
t_{d2}	Delay time, SD3-SD0 write data invalid end to CRC status valid	2	2	Clock Cycles

7.1.3. SDIO Clock Timing

SDIO Clock Timing

Table 5. SDIO Timing requirement

Parameter		Min.	Max.	Unit
f_{clock}	Clock frequency, CLK	0	25	MHZ
DC	Low/high duty cycle	40	60	%
t_{WL}	Pulse duration, CLK low	10		ns
t_{WH}	Pulse duration, CLK high	10		ns
t_{TLH}	Rise time, CLK		4.3	ns
t_{THL}	Fall time, CLK		3.5	ns
t_{ISU}	Setup time, input valid before CLK↑	5		ns
t_{1H}	Hold time, input valid after CLK↑	5		ns
t_{ODLY1}	Delay time, CLK↓ to output valid	0	14	ns
T_{ODLY2}	Delay time, CLK↓ to output invalid	0	14	ns

7.2. Bluetooth HCI Interface

* STR: Start bit;   D0…Dn: Data bits (LSB first);   PAR: Parity bit (if parity is used);   STP: Stop bit

Table 6. BT HCI Timing characteristics

Characteristics	Condition	Symbol	Min	Typ.	Max	Unit
Baud rate	Any rate (1)		37.5	115.2	4000	kbps
Baud rate accuracy	Receive/Transmit	t5/t7			-2.5to+1.5	%
CTS low to TX_DATA on		t3	0	2		us
CTS high to TX_DATA off	Hardware flow control	t4			1	Byte
CTS high pulse width		t6	1			bit
RTS low to RX_DATA on		t1	0	2		us
RTS high to RX_DATA off	Interrupt set to 1/4 FIFO	t2			16	Bytes

Exception for 19.2MHz: Maximum baud rate = 3.84Mbps.

7.3. Bluetooth PCM Interface

Bluetooth can be setting as master or slave mode. For more stable voice performance, slave mode is recommended.
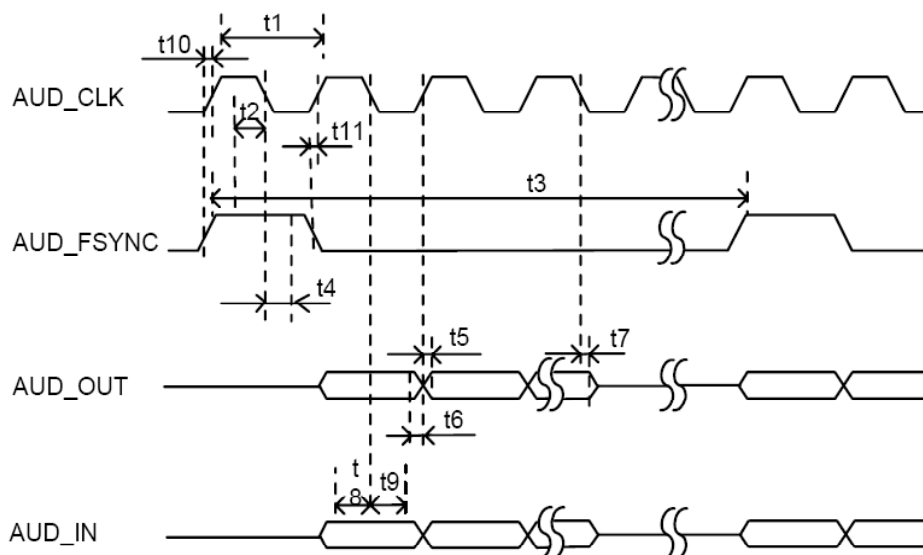
Table 7. BT PCM Slave mode Timing characteristics

Characteristics	Symbol	Min	Typ.	Max	Unit
Master clock frequency	1/t1	64		16000	KHz

		40	50	60	%
Clock duty cycle		40	50	60	%
Synchronization clock frequency	1/t3	1/(8xt1)		1/(65535xt1)	KHz
Synchronization signal width		t1		165545xt1	
Setup time for AUD_FSYNC high to AUD_CLK low	t2	5			ns
Hold time from AUD_CLK low to AUD_FSYNC low	t4	8			ns
Setup time for AUD_IN valid to AUD_CLK low	t8	5			ns
Hold time from AUD_CLK low to AUD_IN invalid	t9	8			ns
Delay time from AUD_CLK high to AUD_OUT data valid	t5			20	ns
Delay time from AUD_CLK low to last data bit of AUD_OUT output set to high impedance	t7			20	ns

8. Debug Interface

The debug interface helps customers to evaluate the HW/SW features for their application. It also helps to debug during the development stage. The WG7351 module support RS232 signals and UART signals for debug purpose. Connect RS232 and UART signals to the test points for future debug support.

8.1. WLAN RS232 Testing Port

"Direct" serial interface (RS232_TX, RS232_RX) used by WLAN TrioScope software package for WLAN RF performance test, debug and manufacturing application.

8.2. Bluetooth HCI Testing Port

HCI_TX and HCI_RX are used by Bluetooth "HCI Tester" software package for Bluetooth RF performance test, debug and manufacturing application.
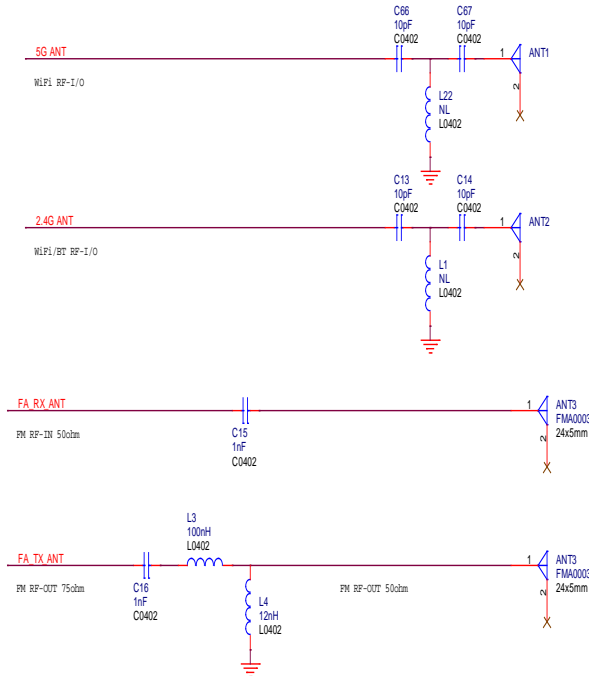
9. Reference Schematic
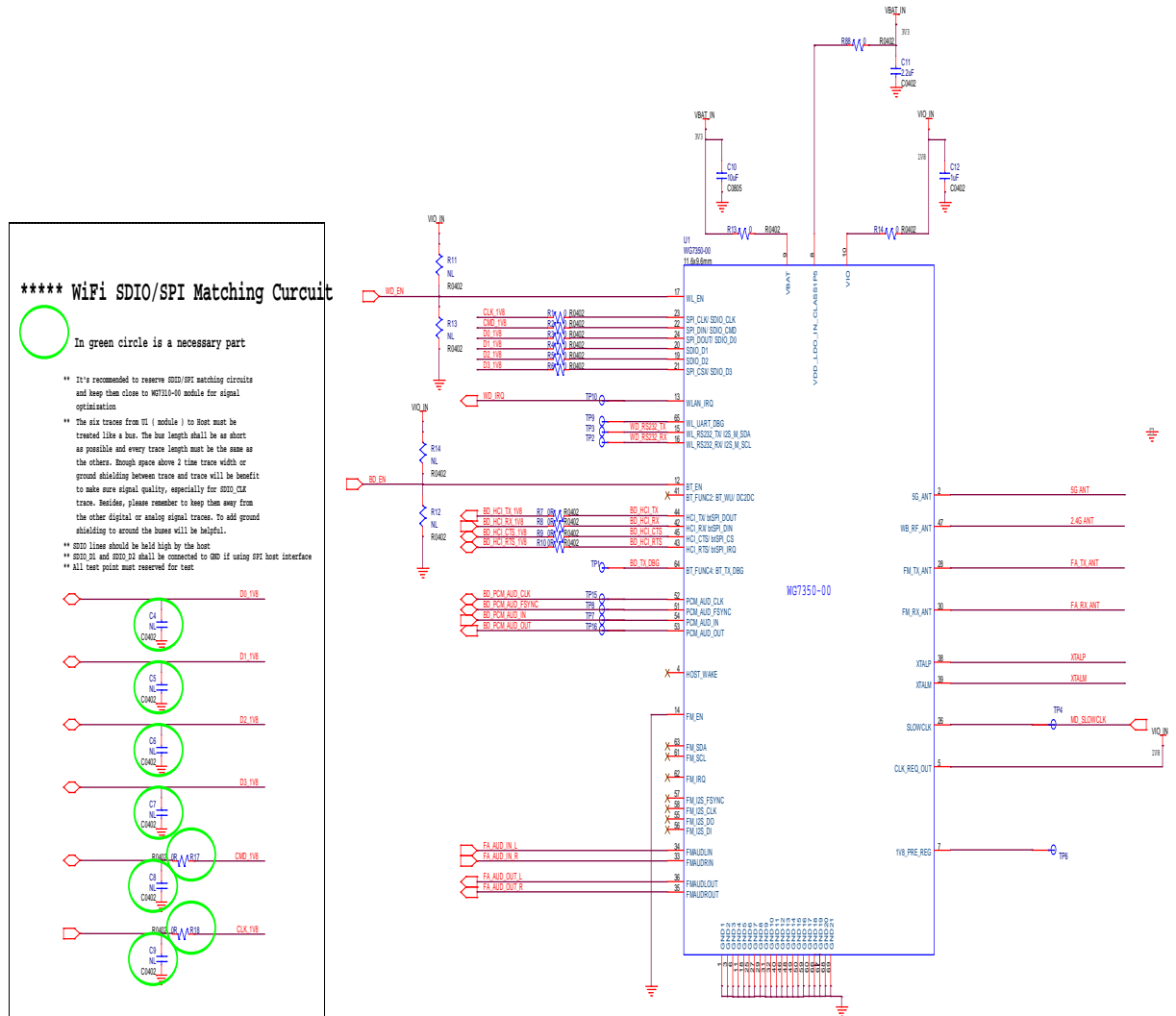
Scheme Brief

WiFi Interface: SDIO or SPI

BT Interface: UART, PCM

FM Interface: UART (with BT together),
Audio IN/OUT

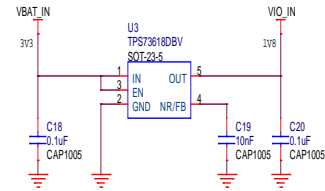Fast Clock: 26MHz or 38.4MHz from outside
Slow Clock: 32.768KHz from outside

** Boot Conditions

VBAT_IN: 2.3~4.8V => 3.3V TYP

VIO_IN: 1.62~1.92V => 1.8V TYP
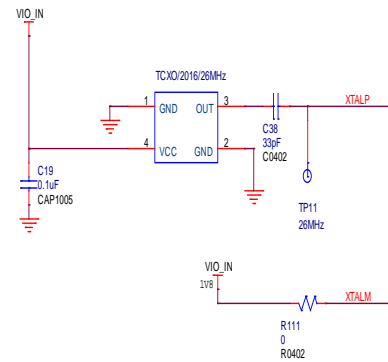
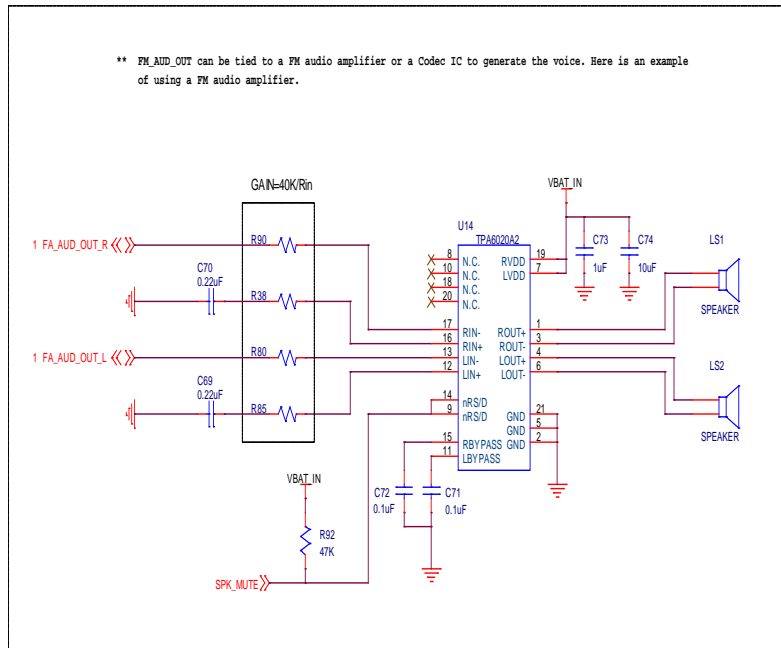Slow Clock: 32.768KHz for module boot
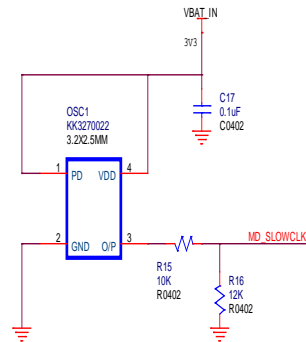and deep sleep

ANTENNA CIRCUITS

1.8V LDO

5G ANT
WiFi RF-I/O

C66 10pF C0402
C67 10pF C0402
L22 NL L0402
ANT1

2.4G ANT
WiFi/BT RF-I/O

C13 10pF C0402
C14 10pF C0402
L1 NL L0402
ANT2

VBAT_IN 3V3
U3 TPS73618DBV SOT-23-5
IN OUT
EN
GND NR/FB
VIO_IN 1V8
C18 0.1uF CAP1005
C19 10nF CAP1005
C20 0.1uF CAP1005

FA_RX_ANT
FM RF-IN 50ohm
C15 1nF C0402
ANT3 FMA0003 24x5mm

26MHz TCXO

FA_TX_ANT
FM RF-OUT 75ohm
C16 1nF C0402
L3 100nH L0402
L4 12nH L0402
FM RF-OUT 50ohm
ANT3 FMA0003 24x5mm

VIO_IN
TCXO/2016/26MHz
GND OUT
VCC GND
C38 33pF C0402
XTALP
C19 0.1uF CAP1005
TP11 26MHz

VIO_IN 1V8
R111 0 R0402
XTALM

1V8 FM AUDIO Output (Option)

** FM_AUD_OUT can be tied to a FM audio amplifier or a Codec IC to generate the voice. Here is an example of using a FM audio amplifier.

32.768K OSC

GAIN=40K/Rin

FA_AUD_OUT_R
C70 0.22uF
R90
R38

FA_AUD_OUT_L
C69 0.22uF
R80
R85

U14 TPA6020A2
N.C. RVDD
N.C. LVDD
N.C.
N.C.
RIN-
RIN+
LIN-
LIN+
ROUT+
ROUT-
LOUT+
LOUT-
nRS/D
nRS/D
GND
GND
RBYPASS GND
LBYPASS

VBAT_IN
C73 1uF
C74 10uF
LS1 SPEAKER
LS2 SPEAKER

VBAT_IN 3V3
OSC1 KK3270022 3.2X2.5MM
PD VDD
GND O/P
C17 0.1uF C0402
R15 10K R0402
R16 12K R0402
MD_SLOWCLK

VBAT_IN
R92 47K
C72 0.1uF
C71 0.1uF
SPK_MUTE

10. Layout Recommendation

10.1. Recommended Trace Layout

● **Digital Signals Layout**

➢ SDIO signals traces (CLK, CMD, D0, D1, D2 and D3) should be routed in parallel to each other and as short as possible. **Besides, every trace length must be the same as the others.** Enough space above 1.5 time trace width or ground shielding between trace and trace will be benefit to make sure signal quality, especially for SDIO_CLK trace. Remember to keep them away from the other digital or analog signal traces. Adding ground shielding around these bus is recommended.

➢ SDIO Clock, Audio Clock (PCM_AUD_CLK), FM I2S Clock (FM_I2S_CLK), FM I2C Clock (FM_SCL), these digital clock signals are a source of noise. Keep the traces of these signals as short as possible. Whenever possible, maintain a clearance around them.

● **RF Trace & Antenna**

➢ 50 ohm trace impedance match on the trace to the antenna.

➢ Recommended 50ohm trace design for PCB layout
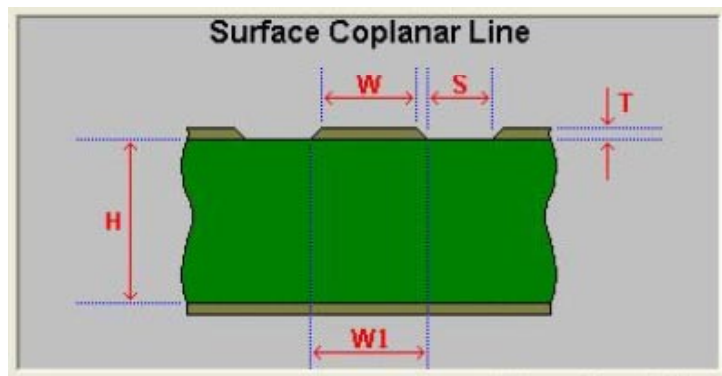
Height Between L1 and L2 **(H):**	10.0 mil
Trace **(W):**	15.35 mil
(W1):	15.35 mil
Thickness **(T):**	2.1 mil
Separation **(S):**	10.0 mil
Dielectric **(Er):**	4.3

➢ Move all the high-speed traces and components far away from the antenna.

➢ Check ANT vendor for the layout guideline and clearance.

➢ Matching circuit layout should be as following figure.
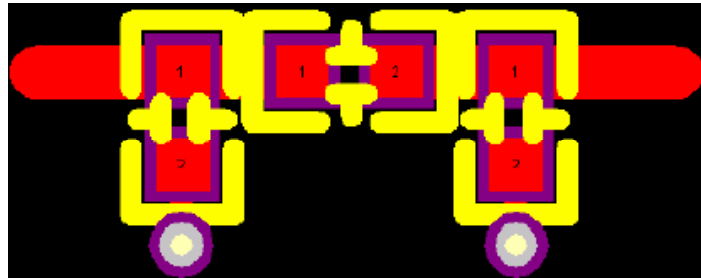
● **Power Trace**

➢ Power trace for VBAT should be 40mil wide. 1.8V trace should be 18mil wide.

● **Ground**

➢ Having a complete Ground and more GND vias under module in layer1 for system stable and thermal dissipation as following figure.

➢ Have a complete Ground pour in layer 2 for thermal dissipation.

➢ Increase the GND pour in the 1st layer, move all the traces from the 1st layer to the inner layers if possible.

➢ Move GND vias close to the pad.
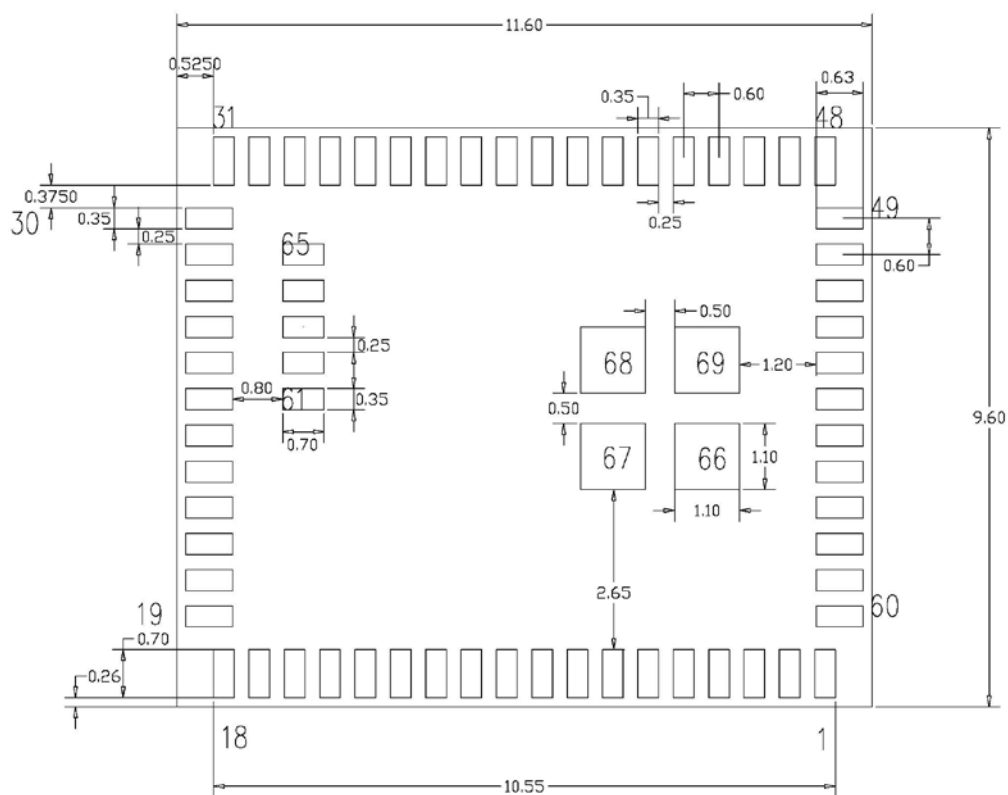
- **Slow Clock**
  - ➢ FM RF module uses the 32-kHz clock, it is extremely important that the slow-clock trace not be routed next to any digital signals.
  - ➢ The slow clock trace should not be routed above or below digital signals on other layers.

11. PACKAGE INFORMATION
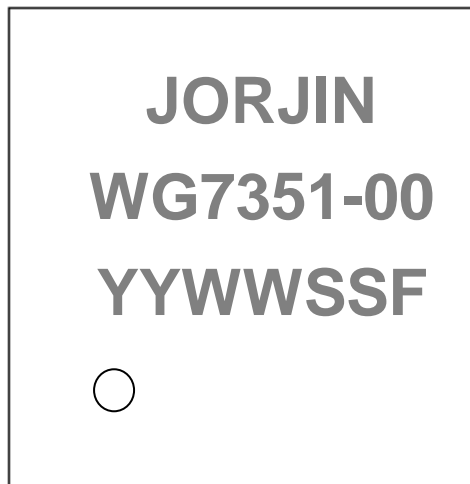
11.1. Module Mechanical Outline
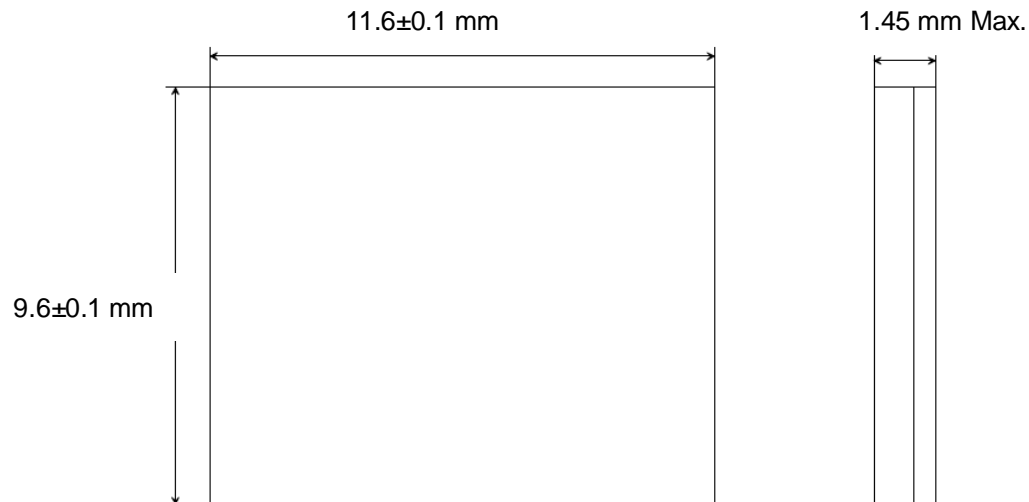
Top View

Bottom View

11.2. Ordering Information

Part number:	WG7351-00

11.3. Package Marking

JORJIN

WG7351-00

YYWWSSF

○

Date Code: **YYWWSSF**

YY = Digit of the year, ex: 2008=08

WW = Week (01~53)

SS = Serial number from 01 ~99 match to manufacture's lot number

F = 1 for Taiwan

12. SMT and Baking Recommendation

12.1. Baking Recommendation

➢ Baking condition：

- Follow MSL Level 4 to do baking process.
- After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be

  a) Mounted within 72 hours of factory conditions <30°C/60% RH, or

  b) Stored at <10% RH.
- Devices require bake, before mounting, if Humidity Indicator Card reads >10%

If baking is required, Devices may be baked for 8 hrs at 125 °C.

12.2. SMT Recommendation

➢ **Recommended Reflow profile：**
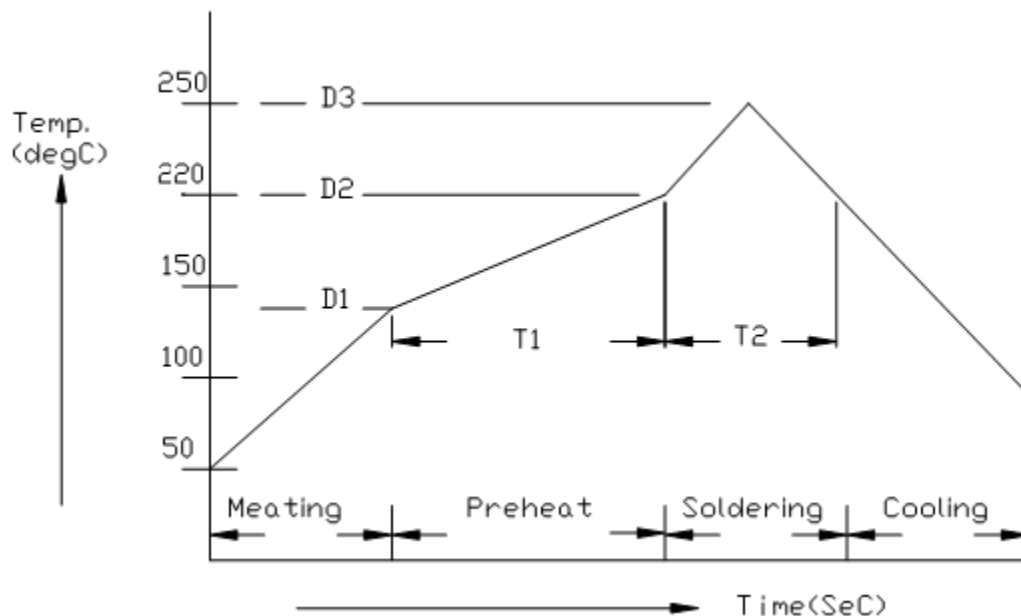
No.	Item	Temperature (°C)	Time (sec)
1	Pre-heat	D1: 140 ~ D2: 200	T1: 80 ~ 120
2	Soldering	D2: = 220	T2: 60 +/- 10
3	Peak-Temp.	D3: 250 °C max	

Note: (1) Reflow soldering is recommended two times maximum.
(2) Add Nitrogen while Reflow process： SMT solder ability will be better.

13. History Change

Revision	Date	Description
R 0.1	2011/12/15	Release 0.1
R 0.2	2011/12/30	Remove SPI interface